FORM PTO-1390 (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	US APPLICATION NO (If known, see 37 CFR 1.5)
OGOH:104	10/018795

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/06330	14 September 2000	28 April 2000 30 June 2000

TITLE OF INVENTION: THIN FILM TRANSISTOR AND METHOD OF PRODUCING THEREOF AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME

APPLICANT(S) FOR DO/EO/US: Yutaka NANNO; Takashi OKADA; Atsunori YAMANO; Kouji SENDA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [x] This express request to begin national examination procedures (35 U.S.C. 371(f) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [ ] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [x] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [x] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [x] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [x] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [x] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [x] Other items or information:
    International Application Publication Cover Page;
    International Search Report;
    PCT Request;
    Forms PCT/IB/301; 304 and 308.

PLEASE ACCEPT THIS AS AUTHORIZATION TO DEBIT OR CREDIT FEES TO DEP. ACCT. 16-0331 PARKHURST & WENDEL

JC08 Rec'd PCT/PTO 21 DEC 2001

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/018795	PCT/JP00/06330	OGOH:104

17. ☒ The following fees are submitted:	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :	
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1,040.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) $710.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	20 - 20 =	0	X $18.00	$
Independent claims	5 - 3 =	2	X $84.00	$ 168.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+$280.00	$

TOTAL OF ABOVE CALCULATIONS =	$ 1,058.00
Reduction of 1/2 for filing by small entity, if applicable. A Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).	$
SUBTOTAL =	$ 1,058.00
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$
TOTAL NATIONAL FEE =	$ 1,058.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$ 40.00
TOTAL FEES ENCLOSED =	$ 1,098.00
Amount to be: refunded	$
charged	$

a. ☒ A check in the amount of $1,098.00 to cover the above fees is enclosed. CK# 14846

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 160331. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO

Roger W. Parkhurst
PARKHURST & WENDEL, L.L.P.
1421 Prince St., Ste. 210
Alexandria, VA 22314-2805
Tel: (703) 739-0220

SIGNATURE

Roger W. Parkhurst
NAME

25,177
REGISTRATION NUMBER

THIN FILM TRANSISTOR AND METHOD OF PRODUCING THEREOF AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME

TECHNICAL FIELD

The present invention relates to a thin film transistor and a method of producing thereof and to a liquid crystal display device utilizing the same.

BACKGROUND ART

First Background Art

Although the driving performance of pixels formed using amorphous silicon (hereinafter referred to as "a-Si") in active matrix-type liquid crystal display devices is sufficiently fulfilled by the a-Si, an external driver circuit (driver) formed using single crystal Si has conventionally been used to drive a panel as it is difficult in terms of performance to form the driver circuit for the signal lines on the same substrate and by the same process.

However, given that the mobility of a-Si is 0.5 $cm^2 \cdot s^{-1} \cdot V^{-1}$ to 1 $cm^2 \cdot s^{-1} \cdot V^{-1}$, with future increases in the number of pixels in liquid crystal panels, the time during which the TFT of a pixel is ON, generally corresponding to at most one row period, will increasingly be reduced, resulting in a deficiency in the performance of writing to the pixels.

On the contrary, by fabricating pixel TFTs using polysilicon (hereinafter referred to as "p-Si"), the performance of the charging of the pixels improves because the mobility of this TFT is higher than that of a

TFT fabricated using a-Si by a factor of 10, 100, or more. Therefore, as the development of high-definition liquid crystal panels progresses, it will be advantageous to form pixel TFTs of p-Si (FPD Expo Forum 97, 2-14).

Generally, there are two types of structures of p-Si TFTs, a top-gate structure wherein the gate electrode is located on the upper side of the channel layer and a bottom-gate structure wherein the gate electrode is on the substrate side of the channel layer. The top-gate structure has an advantage over the bottom-gate structure in terms of miniaturization, as it is possible to fabricate a top-gate TFT having a small parasitic capacitance by doping the TFT with impurities in a self-aligned manner using the gate electrode as the mask.

When a top-gate TFT is used in, for example, a liquid crystal display device and light is applied from the rear surface of the TFT, the channel region of the TFT is irradiated directly by the backlight light. With the irradiation of the channel region by the light, there is the problem of generation of photoconductive current in this region, resulting in an increase in OFF current.

The mechanism of the generation of photoconductive current in semiconductors has been introduced in many articles (for example, Tanaka Kazunobu, ed., *Amorufasu Handōtai no Kiso* (The Basics of Amorphous Semiconductors), 1982), the focus being on solar cells and the like. However, treatments of the mechanism of the generation of photoconductive current in p-Si TFTs are few.

The generation of photoconductive current is generally observed in the form of carrier recombination current that, when an electric field is being

applied, occurs with the creation of electron-hole pairs through the bandgap, the drifting of the electron-hole pairs in response to the electric field, and the increase in majority carriers in each respective region. Under the condition of reverse bias, the channel region, which is below the gate electrode, is such that holes are induced into the area directly below the channel, but the concentration of these carriers is extremely low. On the drain side, it is estimated that the carrier density of electrons, the majority carriers in this region, is approximately $10^{16}/cm^3$ to $10^{18}/cm^3$ when the sheet resistance of the n-region is in the range of from 20 kΩ/□ to 100 kΩ/□. Accordingly, the electrons, which are the majority carriers in the n-region, move toward the channel side and diffuse to form a diffusion potential Vd. It should be noted that Wd represents the width of the depletion layer.

By irradiation with light, electron-hole pairs are generated in this depleted region. The generated electron-hole pairs are both attracted to the electric field such that the electrons migrate in the direction of the drain and the holes migrate in the direction of the channel. The electrons having migrated to the drain side and the holes having migrated to the channel side recombine and disappear at each respective region. The electric charge consumed by this recombination is supplied from the source and the drain electrodes respectively and is observed as photoconductive current.

When the OFF current is increased (degradation of OFF characteristics) due to such photoconductive current, the following problems arise.

Image quality degradation caused by the degradation of OFF characteristics takes the form of luminance gradation and crosstalk. As

shown in Fig. 38(a), luminance gradation is caused by differing current/luminance characteristics of the liquid crystal in the upper portion and lower portion of the screen, resulting in a discrepancy in the luminance of the upper portion and lower portion of the screen. Crosstalk, on the other hand, is an occurrence as shown in Fig. 38 (b) wherein when a black box pattern is displayed in the central portion of white, the black image leaves a tail in the vertical or horizontal directions. In addition, other occurrences of degradation of OFF characteristics such as an increase in flicker and the generation of unevenness in luminance have a considerable effect on image quality.

Second Background Art

Because p-Si TFTs have high mobility, it is possible to form both active matrix elements and part or the whole of the signal driver circuit on a glass substrate in the screen. However, compared with a-Si TFTs and MOS field effect transistors, p-Si TFTs have the drawback of a large OFF current.

In order to reduce this OFF current, a method is carried out, as disclosed in Japanese Unexamined Patent Application Publication H5-136417, wherein a low concentration impurity region (LDD region) is provided adjacent to at least one of the source region and the drain region of the TFT (the first prior art method).

As another method of forming LDD regions, a method of controlling the presence of TaOx in LDD regions has been disclosed (Euro Display, '96, p. 547, the second prior art method).

As for the mechanism that makes LDD regions effective for reducing the OFF current, it is thought that, as is disclosed in the Japanese

Unexamined Patent Application Publication 5-136417, the electric field across the junctions of the channel/LDD regions is reduced in comparison to cases where LDD regions are not provided because the LDD regions have a resistance higher than that of the drain region.

In both the two methods described above, portions having differing doping concentrations are formed by the presence or absence of TaOx by aligning the LDD regions with a mask or by the presence or absence of a resist film. In these methods, in order to be certain that LDD regions are obtained, it is necessary to ensure that the length of the LDD regions is a length equal to or greater than the dimensional tolerance of the mask alignment.

In contrast to these methods, there is a third prior art method, as is described in Japanese Unexamined Patent Application Publication H7-140485, wherein LDD regions are formed self-aligned to the gate electrode. According to the present method, Al oxide layers are formed on side surfaces of the gate electrode by carrying out anodic oxidation on the Al that is to become the gate electrode, and an n-type or p-type impurity element is introduced using this as a mask, making it possible to fabricate lightly doped layers having a thickness approximately equal to that of the source region, the drain region, and the oxide layers on the side surfaces of the gate electrode.

By employing this method, it is made possible to form LDD regions self-aligned to the gate electrode, eliminating the need for a mask in forming the LDD regions and to form regions having a high impurity concentration to a fairly short length of from 0.1 μm to 0.5 μm, which

corresponds to the thickness of the oxide present on the side surfaces of the anodically oxidized Al.

Although the LDD structure is highly effective for the reduction of OFF current, there is, in the ON state, in which current flows through the channel below the gate electrode of the TFT, the drawback of a drop in ON current because the LDD regions, comparatively high resistance layers, are inserted in series with the channel region.

LDD regions essentially have a higher resistance than those of source and drain regions, and there has been a tendency for the effects of this resistance to become very noticeable, as the characteristics of TFTs have improved. Thus, it is necessary that LDD regions, which are high resistance regions, have a length such that OFF current is sufficiently reduced and have a resistance value low enough to ensure a high ON current.

However, at the present, there is no method for determining a guideline for the length of the LDD regions, making it necessary to ensure LDD regions having a length longer than is necessary. Generally, it is necessary to secure LDD regions having a length longer than 1.5 μm, which is accordingly a cause of a drop in the ON current of a TFT.

In addition, while employing the method described in the third prior art example makes it possible to form LDD regions to a fairly short length of from approximately 0.1 μm to 0.5 μm, in general, when the resulting TFT is used for a driver TFT or a pixel TFT of a liquid crystal panel, the driving voltage is from approximately 5 V to 15 V, fairly high voltages compared to common ICs. Therefore, when the length of LDD regions is from 0.1 μm to

0.5 μm, the advantageous effect is insufficient, making it impossible to sufficiently reduce OFF current by the present process.

In consideration of the foregoing problems, it is a first object of the present invention to provide a thin film transistor that suppresses image quality degradation such as luminance gradation and crosstalk and realizes high performance and high reliability by utilizing a structure that suppresses OFF current (photoconductive current) during light irradiation.

It is a second object to provide a thin film transistor that realizes high performance and high reliability by utilizing a structure that, along with suppressing OFF current, minimizes the length of the LDD regions to suppress a decrease in ON current.

DISCLOSURE OF THE INVENTION

In order to solve the foregoing problems, a first aspect of the invention provides a thin film transistor comprising a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, and a drain region, the source region and the drain region disposed on either side of the channel region, wherein a depletion layer is formed between the channel region and the drain region, and the width of the depletion layer and photoconductive current are in a proportional relationship, the photoconductive current generated when the channel region is irradiated with light, and the width of the depletion layer is equal to or less than a value obtained on the basis of the proportional relationship so that the photoconductive current falls within a range of specified permissible values.

As described above, it was discovered that there is a proportional relationship between depletion layer width and photoconductive current, and based on this discovery, the keeping of photoconductive current at or less than a permissible value by controlling the depletion layer width was achieved, thereby making it possible to provide a thin film transistor that does not bring about image quality degradation such as luminance gradation and crosstalk.

A second aspect of the invention provides a thin film transistor according to the first aspect wherein the relationship of expression (1)

(1)

$$(R+30)\cdot W < A$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region and W (μm) is the channel width of the channel region. Note that A is a constant determined by photoconductive current and light intensity.

A third aspect of the invention provides a thin film transistor according to the second aspect wherein the relationship of expression (2)

(2)

$$(R+30)\cdot W < 1\times 10^{3}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region and W (μm) is the channel width of the channel region.

As shown in the expressions (1) and (2) above, by means of the relationship between the new controlling factor (the sheet resistance of the drain region) and the channel width of the channel region, it is possible to regulate the range in which OFF current (photoconductive current) is suppressed during irradiation of light. Because a thin film transistor that

satisfies the relationships of expressions (1) and (2) suppresses an increase in OFF current during the irradiation of light, crosstalk and luminance gradation are prevented, and high performance and high reliability thereby realized.

A fourth aspect of the invention provides a thin film transistor according to the third aspect, wherein the channel width W of the channel region is 2 μm or less.

The relationship of expression (2) is such that even in cases in which the channel width of the channel region is 2 μm or less, an increase in OFF current during the irradiation of light is suppressed by the sheet resistance R and the channel width W.

A fifth aspect and sixth aspect of the invention provide thin film transistors according to the third aspect and the fourth aspect, respectively, wherein the sheet resistance of the drain region is in the range of from 20 kΩ/□ to 100 kΩ/□.

The sheet resistance is restricted to the above range in this way since OFF current suddenly increases when the sheet resistance is 20 kΩ/□ or lower and ON current of the transistor decreases when the sheet resistance is 100 kΩ/□ or higher, making the operation of a panel unstable. By making the sheet resistance of the drain region in the range of from 20 kΩ/□ to 100 kΩ/□, a thin film transistor is provided wherein, while a reduction of OFF current is realized, a decrease in ON current does not occur.

A seventh aspect of the invention provides a thin film transistor for use as a switching element of a liquid crystal display device, the thin film

transistor comprising a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, and a drain region, the source region and the drain region disposed on either side of the channel region, wherein a low concentration impurity region having an impurity concentration less than that of the source region and the drain region is formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, and the length ΔL of the low concentration impurity region is 1.0 μm or less, the luminance of a backlight of the liquid crystal display device being 2000 (cd/m^2) or higher.

In this way, by forming a low concentration impurity region, the spreading of the depletion layer is kept within the range of the low concentration impurity region, which has a length ΔL of 1.0 μm or less, and a thin film transistor in which photoconductive current (OFF current) does not increase is realized.

An eighth aspect of the invention provides a thin film transistor comprising a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being disposed on either side of the channel region and the low concentration impurity region being formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein, the relationship of expression (3)

(3)

$$\Delta L > (W \cdot Vlc)/36$$

is satisfied, where ΔL (μm) is the length of the low concentration impurity region, Vlc (V) is the source-drain voltage, and W (μm) is the channel width of the channel region.

By the satisfying of such a relationship, when the thin film transistor is OFF, a reduction in OFF current is realized because the low concentration impurity region becomes a high resistance layer that is drained of carriers. In addition, a guideline for the length of the LDD region can be determined from the expression (1), eliminating the need to ensure an LDD region having a length that is longer than necessary for the reduction of OFF current.

A ninth aspect of the invention provides a thin film transistor according to the eighth aspect wherein the relationship of expression (4)

(4)

$$\Delta L < 1.5 \cdot (W / L)$$

is satisfied, where L (μm) is the channel length of the channel region.

By further satisfying such an expression, when the transistor is on, electrons that serve as carriers gather in the low concentration impurity region under the gate electrode in response to the electric field of the gate electrode and a reduction in ON current does not occur. Thus, it is made possible to hold OFF current to a small value while ensuring sufficient ON current.

A tenth aspect of the invention provides a thin film transistor according to the ninth aspect, wherein the channel width W (μm) of the

channel region is 2 μm or less.

In this way, by regulating the length ΔL of the low concentration impurity region, a decrease in ON current does not occur while a reduction in OFF current is realized.

An eleventh and twelfth aspect of the invention provide thin film transistors according to the ninth aspect and tenth aspect, respectively, wherein the sheet resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.

A thirteenth aspect of the present invention provides a thin film transistor according to claim 11, wherein the low concentration impurity region is formed only in the region between the drain region and the channel region.

The provision of a low concentration impurity region is essentially for the purpose of relaxing the effect of the electric field on the drain region, and from this standpoint, it is not necessary to provide a low concentration impurity region in both the drain region and the channel region. Supposing a low concentration impurity region is formed in at least one of a region between the drain region and the channel region and a region between the drain region and the channel region, it is made possible to reduce the area of the thin film transistor.

A fourteenth aspect of the invention provides a liquid crystal display device comprising a liquid crystal panel portion comprising thin film transistors serving as switching elements, each of the thin film transistors being a thin film transistor of claim 1 and a backlight portion for supplying light from a rear surface side of the liquid crystal panel portion, wherein the

relationship of expression (5)

(5)

$$(R+30)\cdot B\cdot W < C$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the luminance of the backlight portion, and W (μm) is the channel width of the channel region. It should be noted that C is a constant determined by the photoconductive current.

A fifteenth aspect of the invention provides a liquid crystal display device according to the fourteenth aspect, wherein the relationship of expression (6)

(6)

$$(R+30)\cdot B\cdot W < 1\times 10^6$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the luminance of the backlight portion, and W (μm) is the channel width of the channel region.

A sixteenth aspect of the invention provides an EL display device comprising a light-emitting layer and a counter electrode formed thereon, the light-emitting layer being on a pixel electrode upper layer formed on a substrate having thin film transistors, the display device wherein, each of the thin film transistors is a thin film transistor of claim 1, and the relationship of expression (5)

(5)

$$(R+30)\cdot B\cdot W < C$$

is satisfied, where B (cd/m^2) is the light intensity of light applied to a channel region of each of the thin film transistors. It should be noted that

C is a constant determined by the photoconductive current.

A seventeenth aspect of the invention provides an EL display device according to the sixteenth aspect, wherein the relationship of the expression (6)

$$(R+30)\cdot B\cdot W<1\times10^{6} \quad (6)$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the light intensity of light applied to the channel region, and W (μm) is the channel width of the channel region.

An eighteenth aspect of the invention provides a method of producing a thin film transistor, comprising the steps of forming a polycrystalline silicon semiconductor layer on an insulating substrate, forming a gate insulating film on the polycrystalline silicon semiconductor layer, forming a gate electrode in a pattern on the gate insulating film, carrying out anodic oxidation by oxidizing a side surface of the gate electrode to form a metal oxide film covering the side surface of the gate electrode, and doping the polycrystalline silicon semiconductor layer with impurities, the gate electrode being used as a mask, wherein the thickness of the metal oxide film formed in the step of carrying out anodic oxidation is controlled to make the length ΔL of a low concentration impurity region formed in the step of carrying out impurity doping 1.0 μm or less.

A nineteenth aspect of the invention provides a method of producing a thin film transistor, comprising the steps of forming a polycrystalline silicon semiconductor layer on an insulating substrate, forming a gate insulating film on the polycrystalline silicon semiconductor layer, forming a gate

electrode in a pattern on the gate insulating film, carrying out a first impurity doping by doping the polycrystalline silicon semiconductor layer with impurities, using the gate electrode as a mask; forming a masking film on a semiconductor region doped with impurities in the step of carrying out a first impurity doping, the masking film being formed in a pattern by anisotropic etching, carrying out a second impurity doping by doping the polycrystalline silicon semiconductor layer with impurities using the masking film as a mask so that an impurity concentration difference exists between a region under the masking film and regions other than the region under the masking film, whereby a low concentration impurity region having an impurity concentration lower than that of the source region and the drain region is formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region and by making the length of the low concentration impurity region 1.0 μm or less.

A twentieth aspect of the invention provides a thin film transistor according to claim 19, further comprising a step of inspecting by designating the thin film transistor having a low concentration impurity region with a length ΔL of 1.0 μm or less a quality product.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1(a) and 1(b) are graphs showing the relationship between the channel width W of a channel region in a TFT and photoconductive current (OFF current: I_{OFF}), and a graph showing the relationship between backlight luminance and photoconductive current.

Fig. 2(a) and 2(b) are graphs showing the results of a simulation of an electric field when a TFT is in the OFF state.

Fig. 3 is a graph showing the relationship between sheet resistance and depletion layer width obtained through a simulation.

Fig. 4 is a graph showing the results of measuring the relationship between depletion layer width and photoconductive current at a sheet resistance corresponding to the depletion layer width, the depletion layer width being obtained through a simulation where W= 4 μm.

Fig. 5 is a diagram showing an equivalent circuit of the active matrix.

Fig. 6 is a graph showing the results of a simulation of voltage loss in a pixel.

Fig. 7 is a schematic cross sectional view of a liquid crystal display device utilizing a thin film transistor as the pixel switching element in accordance with embodiment1-1 of the present invention.

Fig. 8 is a schematic cross sectional view of a thin film transistor in accordance with embodiment1-1 of the present invention.

Fig. 9 is a schematic plan view of Fig. 8.

Fig. 10(a) to 10(h) are schematic cross sectional views showing a method of producing a thin film transistor in accordance with embodiment 1-1 of the present invention.

Fig. 11(i) to 11(m) are schematic cross sectional views showing the same method of producing a thin film transistor.

Fig. 12 is a flow chart showing the same method of producing a thin film transistor.

Fig. 13 is a graph showing the voltage-current characteristics of thin

film transistors.

Fig. 14 is a graph showing the variation in OFF current within the area of a substrate.

Fig. 15 is a graph showing the results of a simulation of the Vg-Id characteristics of a thin film transistor with the concentration of the n− type region as the parameter.

Fig. 16(a) and 16(b) are graphs showing the results of a simulation of an electric field when a TFT is in the OFF state.

Fig. 17(a) to 17(g) are schematic cross sectional views showing a method of producing a thin film transistor in accordance with embodiment 1-2 of the present invention.

Fig. 18(h) to 18(j) are schematic cross sectional views showing the same method of producing a thin film transistor.

Fig. 19 is a plan view showing the wiring pattern of a C-MOS inverter that utilizes thin film transistors in accordance with embodiment 1-3 of the present invention.

Fig. 20 is a diagram of the equivalent circuit of the C-MOS inverter.

Fig. 21 is a cross sectional view of Fig. 19 taken along line X-X' of Fig. 19.

Fig. 21 is a cross sectional view of Fig. 19.

Fig.22 is a graph showing the points of operation of a C-MOS inverter during on/off when an n-channel transistor is biased.

Fig. 23(a) to 23(d) are graphs showing the results of a simulation of Vg-Id characteristics when the length of the LDD region, the sheet resistance being the parameter, is changed from 0.5 μm to 3 μm.

Fig. 24(a) and 24(b) show the results of a simulation of an electric field in a channel region and an LDD region when a TFT is in the OFF state (Vg=−10V and Vd=6V).

Fig. 25(a) and 25(b) are graphs showing, in an actual TFT having an LDD region, the relationship between the length (ΔL) of the LDD region and OFF current and the relationship between the length (ΔL) of the LDD region and ON current.

Fig. 26 is a simplified cross sectional view of a thin film transistor in accordance with embodiment 2-1 of the present invention.

Fig. 27 is a schematic plan view of Fig. 26.

Fig. 28(a) to 28(h) are schematic cross sectional views showing a method of producing a thin film transistor in accordance with embodiment 2-1 of the present invention.

Fig. 29(a) to 29(e) are schematic cross sectional views showing a method of producing a thin film transistor in accordance with embodiment 2-1 of the present invention.

Fig. 30 is a flow chart showing a method of producing a thin film transistor in accordance with embodiment 2-1 of the present invention.

Fig. 31(a) to 31(d) are schematic cross sectional process diagrams illustrating the process of forming LDD regions.

Fig. 32 is a perspective view of a photomask and a substrate.

Fig. 33(a) and 33(b) are plan views of the same.

Fig. 34(a) and 34(b) are schematic cross-sectional views of a thin film transistor after the formation of LDD regions.

Fig. 35 is a graph showing the voltage-current characteristics of a thin

film transistor in accordance with embodiment 2-1.

Fig. 36 is a graph showing the variation in OFF current with the area of a substrate of a thin film transistor in accordance with embodiment 2-1.

Fig. 37 is a graph showing of a simulation of the Vg-Id characteristics of a thin film transistor, the concentration of the LDD regions being the parameter.

Fig. 38(a) and 38(b) are schematic diagrams illustrating luminance gradation and crosstalk.

BEST MODE FOR CARRYING OUT THE INVENTION

First Invention Group

General Concepts of the first invention group

After an explanation of the general concepts of the first invention group, the specific embodiments will be explained with reference to the figures.

An object of the first invention group is to suppress photoconductive current when a TFT is irradiated with light.

In order to achieve the above-mentioned object, the present inventers searched for parameters that have a correlation with photoconductive current and as a result, discovered that there is a proportional relationship between depletion layer width and photoconductive current. Controlling (reducing) the depletion layer width according to this proportional relationship makes it possible to keep the photoconductive current at or less than a permissible value and to thus provide a thin film transistor that does not bring about image quality degradation such as luminance gradation and

crosstalk.

It should be noted that the "depletion layer width" is defined as the distance between the respective tangent lines of the two points of sudden shift in the rate of change of electric field intensity as shown in Fig. 2(a), which is described later.

It has been known that there is a correlation between backlight luminance B and photoconductive current and between channel width W of a channel region and photoconductive current, and TFTs have been designed based on these two control parameters. However, for the suppressing of photoconductive current, errors sometimes arise in the designing of a TFT as it is not sufficient to use only these two control parameters.

In consideration of this, the present inventors again thoroughly considered the "proportional relationship between depletion layer width and photoconductive current" and discovered that there is also a correlation between the sheet resistance of a drain region and photoconductive current. Thus, by making the additional factor of sheet resistance R a basis for evaluation, the control parameters become three. In comparison to prior art examples in which there were two control parameters, accuracy in the designing of a thin film transistor improves, and it becomes possible to suppress photoconductive current to a great degree. In the following, the relationship between depletion layer width and photoconductive current is first explained, and then the relationship between backlight luminance B, the sheet resistance R of a drain region, and the channel width W of a channel region is explained. Finally, the fundamentals of specific

techniques of fabricating a TFT for suppressing photoconductive current are explained.

First, the present inventors, along with measuring the relationship between the channel width of the channel region in a TFT and photoconductive current, measured the relationship between the sheet resistance of a drain region and photoconductive current. Next, by simulations, the present inventors carried out operation analysis and obtained a range of depletion layer widths.

Fig. 1(a) is a graph showing the relationship between the channel width W of the channel region in a TFT and photoconductive current (OFF current: I_{OFF}). The relationship between the channel width W and photoconductive current I_{OFF} is shown when light is applied, light that is 6000 cd/cm^2 as represented by the solid line, 4000 cd/cm^2 as represented by the dashed line, and 2000 cd/cm^2 as represented by the dot-dash line.

From Fig. 1(a), it is clear that during light irradiation, OFF current I_{OFF} is proportional to channel width W. Fig. 1(b) is a graph showing the relationship between backlight luminance and photoconductive current; it could be confirmed that OFF current I_{OFF} is proportional to backlight luminance B.

Fig. 2(a) is a graph showing the results of a simulation of an electric field when a TFT is in the OFF state. From the results of the simulation shown in Fig. 2(a), it is understood that the electric field is almost completely concentrated in the junction portion of the channel/drain regions, and when the sheet resistance of an LDD region is 20 kΩ/□ (solid line), the depletion layer width is about 0.5 μm, this depletion layer region extending

mostly into the channel side. By contrast, it is confirmed that when the sheet resistance is 100 kΩ/□ (dashed line), the depletion layer width is about 0.9 μm and spreads into the LDD region.

Based on this, it was discovered that by changing sheet resistance, depletion layer width also changes. At this point, the present inventors investigated the relationship between sheet resistance and depletion layer width. The results are shown in Fig. 3. Fig. 3 shows the relationship between sheet resistance and depletion layer width obtained through a simulation. It is confirmed that depletion layer width Wd is proportional to sheet resistance R. It is thought that this is because the depletion layer extends into regions with low carrier concentration, as is the case with the spreading of a depletion layer in a p-n junction. The relationship between sheet resistance and depletion layer width shown in Fig. 3 is represented by the expression (7) below.

(7)

$$Wd = 8\times10^{-3}\cdot R + 0.24$$

Fig. 4 shows the results of measuring the relationship between depletion layer width and photoconductive current at a sheet resistance corresponding to the depletion layer width, the depletion layer width being obtained through a simulation where W=4 μm.

When depletion layer width and photoconductive current are plotted by their respective logarithms, a straight line with a slope of approximately 1 is obtained. This suggests that photoconductive current is a brought about by the depletion layer region. The relationship between depletion layer width Wd and photoconductive current is represented by the expression (8) below.

(8)

$$I_{photo} = 5 \times 10^{-15} \cdot Wd$$

In the expression (8) above, I_{photo} is the amount of photoconductive current per 1 cd/m^2 of light intensity when the channel width is 4 μm.

From the expression (8) above, it was discovered that there is a proportional relationship between depletion layer width Wd and photoconductive current I_{photo}. Controlling (reducing) the depletion layer width according to this makes it possible to keep the photoconductive current at or less than a permissible value and to thus provide a thin film transistor that does not bring about image quality degradation such as luminance gradation and crosstalk and that realizes high performance and high reliability. It should be noted that a "permissible value" is a value of, for example, 10 pA or less as will be discussed later.

In addition, as is understood from Fig. 1(a), because I_{off} is proportional to channel width W and to light intensity B, I_{off} and I_{photo} satisfy the relationship shown in the expression (9) below.

(9)

$$I_{off} = I_{photo} \cdot (W/4) \cdot B$$

Therefore, when I_{photo} is eliminated from the above expression (9) and expression (8), the expression (10) below results.

(10)

$$I_{off}[4/(W \cdot B)] = 5 \times 10^{-15} \cdot Wd$$

Then, when depletion layer width Wd is eliminated from the above

expressions (7) and (10), the expression (11) below is obtained. As is understood from Fig. 1(a), I_{off} is proportional to channel width W.

(11)

$$R = I_{off} \cdot 10^{17} / (B \cdot W) - 30$$

However, in order to maintain high image quality, it is generally necessary that the value of I_{off} be 10 pA or less. The reason for this is explained below. Fig. 5 shows an equivalent circuit of an active matrix.

As the OFF resistance R_{off} of a TFT decreases, it becomes impossible to maintain an electric charge until the next writing, resulting in voltage loss. The pixel voltage V after time T has elapsed is as represented by expression (12).

(12)

$$V = V_0 \{1 - \exp[T / (R_{off} \times Ctot)]\}$$

Note that Ctot=Cs+Clc.

Making the OFF current ($R_{off}=V_{sd}/I_{off}$) of a TFT a parameter, the results of a simulation of time and voltage loss are shown in Fig. 6. From Fig. 6, it is confirmed that with a hold time of 16 msec (1/60 Hz), in order to keep voltage loss to 0.02 V or less, it is necessary that OFF current be 10 pA or less when light from the backlight is being applied.

Thus, when I_{off} in the expression (11) is 10 pA or less, the following expression is obtained.

(6)

$$(R+30) \cdot B \cdot W < 10 \cdot 10^{-12} \cdot 10^{-17} = 1 \times 10^{6}$$

Because the value that suppresses the OFF current varies depending

on the conditions under which a thin film transistor is used, this relationship can be represented by the expression (5) below.

$$(R+30)\cdot B\cdot W < C \tag{5}$$

It should be noted that C is a constant determined from the photoconductive current.

In such a manner, a thin film transistor that satisfies the above expression (6) can suppress photoconductive current, and therefore, it is made possible to prevent crosstalk and luminance gradation and to realize excellent image quality, high performance, and high reliability.

Although the above expression (6) includes backlight luminance of a liquid crystal panel, in general the thin film transistor is not limited to use only in a transmissive-type display provided with a backlight. Therefore, supposing backlight luminance is at the highest, 5000 cd/m^2, the expression (6) becomes

$$(R+30)\cdot W < 2\times 10^2 \tag{2'}$$

and a thin film transistor satisfying the above expression (2') can be achieved without relation to the backlight luminance B, in other words regardless of whether the thin film transistor is used in a transmissive-type or reflective-type display.

It should be noted that a thin film transistor satisfying the above expression (2') can provide better performance if the expression (2) below is also satisfied.

(2)

$$(R+30)\cdot W<1\times10^{3}$$

It is also possible to represent the expression (11) as in expression (11') below.

(11')

$$(R+30)\cdot W<(I_{off}\cdot10^{-17})/B$$

When constant A, determined by I_{off} and B, is substituted for the right side of the above expression (11'), expression (11') may be represented by the expression (1) below:

(1)

$$(R+30)\cdot W<A$$

where A is a constant determined by photoconductive current and light intensity.

Moreover, in the foregoing structure of a TFT, by forming an LDD region, it is possible to suppress the photoconductive current, which as described earlier is proportional to the depletion layer width, without the depletion layer spreading beyond the LDD region. Fig. 16(a) and 16(b) show the results of a simulation of an electric field in the channel region and an LDD region when a TFT is in the OFF state (when V_g=−10V and V_d=6V).

From the results of this simulation, it was confirmed that the region exposed to an electric field is dependant on sheet resistance. When the sheet resistance of the LDD region is 20 kΩ/□, the depletion layer width is about 0.4 μm, and when the sheet resistance is 100 kΩ/□, the depletion layer width is about 1.0 μm.

It should be noted that the foregoing was carried out with the channel width at 4 μm, but that when the channel width of the channel region is miniaturized to 2 μm or less, the relational expressions (1) and (2) are especially effective guidelines for the fabrication of a thin film transistor.

In the following embodiments, the fabrication of a TFT is specifically described based on the foregoing simulations.

Embodiment 1-1

Fig. 7 is a schematic cross sectional view of a liquid crystal display device utilizing as the pixel switching element a thin film transistor in accordance with embodiment 1-1 of the present invention, Fig. 8 is a schematic cross sectional view of a thin film transistor in accordance with embodiment 1-1 of the present invention, and Fig. 9 is a schematic plan view of Fig. 8.

As shown in Fig. 7, a liquid crystal display device 50 is a transmissive-type liquid crystal display device provided with a liquid crystal panel portion 51, a backlight portion 52 disposed on the rear surface side of the liquid crystal panel 51, and the like. The liquid crystal panel portion 51 comprises polarizing plates 53 and 53, glass substrates 2 and 54b, thin film transistors 1 arranged in a matrix, pixel electrodes 55, orientation films 56, a liquid crystal layer 57, a common electrode 58, and the like.

The thin film transistors 1 (hereinafter referred to as TFTs) and the pixel electrodes 55 are formed on the glass substrate 2, and the common electrode 58 is formed on the substrate 54b. The orientation films 56 and 56 composed of polyimide resin are formed on the substrates 2 and 54b respectively, the orientation films 56 and 56 having undergone rubbing

treatment beforehand such that the orientation directions of the orientation films are perpendicular to one another, and the glass substrates 2 and 54b are positioned facing each other with spacers, not shown in the figure, disposed therebetween.

The liquid crystal layer 57 is sandwiched between the substrates 2 and 54b, and liquid crystal in the liquid crystal layer 57 is set to a twist of 90°. The polarizing plates 53 and 53 are arranged on the outer surfaces of the substrates 2 and 54b so that the angles of vibration of light that passes through the polarizing plates are parallel to one another.

The backlight portion 52 is disposed on the rear (lower) side of the liquid crystal panel portion 51. The backlight portion 52 comprises a light-emitting element such as a cold-cathode tube, a light scattering plate for uniformly distributing light, and the like.

The thin film transistor is now described using Figs. 8 and 9.

The thin film transistor 1 is constructed such that a polycrystalline silicon layer 3 having a thickness of 500 Å, a gate insulating layer 4 composed of SiO_2 (silicon dioxide) and having a thickness of 1000 Å, a gate electrode 5a composed of aluminum, and an interlayer insulating layer 6 composed of SiO_2, are stacked on the glass substrate 2 in that order.

The polycrystalline silicon layer 3 comprises a channel region 3c located directly below the gate electrode 5a, a source region 3a (n+ layer) having a high impurity concentration, and a drain region (n+ layer) 3b having a high impurity concentration. In the present embodiment, the length ΔL of LDD regions (n− layer) 3d and 3e is fixed at 0.4 μm. The channel width W of the channel region 3c is fixed at 5 μm.

The TFT is designed such that the expression (6) below is satisfied where the sheet resistance of the drain region is R (kΩ/□), the luminance of the backlight portion 52 of the liquid crystal display device 50 using the active matrix TFT is B (cd/m^2), and the channel width of the channel region 3c is W (μm).

(6)

$$(R+30)\cdot B\cdot W = I_{off} < 1\times 10^{6}$$

In TFT 1, a source electrode 7 and a drain electrode 8 composed of, for example, aluminum are also provided. The source electrode 7 is connected to the source region 3a by a contact hole 9a which is formed in the gate insulating layer 4 and the interlayer insulating layer 6, and the drain electrode 8 is connected to the drain region 3b via a contact hole 9b which is formed in the gate insulating layer 4 and the interlayer insulating layer 6.

A method of producing a thin film transistor is now described. Fig. 10(a) to 10(h) are schematic cross sectional views showing a method of producing a thin film transistor in accordance with embodiment1-1 of the present invention, Fig. 11(i) to 11(m) are schematic cross sectional views showing the same method of producing a thin film transistor, and Fig. 12 is a flow chart showing the same method of producing a thin film transistor.

(1) First, an a-Si layer 15 having a film thickness of 500 Å is deposited on the glass substrate 2 by plasma CVD, and dehydrogenation is carried out at 400°C (Fig. 10(a)). The purpose of this dehydrogenation is to prevent ablation of the Si film by the desorption of hydrogen when crystallization is carried out. For the step of forming the a-Si, in addition to plasma CVD, it is also possible to utilize processes such as reduced pressure CVD and

sputtering. Moreover, by utilizing these methods such as the plasma CVD method, a polysilicon film can be directly deposited on the substrate. In these cases, the need for a laser-annealing step discussed later is eliminated.

(2) The melting and recrystallization (transformation into p-Si) of the a-Si layer 15 is then carried out by laser annealing utilizing an excimer laser having a wavelength of 308 nm to form a polycrystalline silicon layer 16 (Fig. 10(b)).

(3) The polycrystalline silicon layer 16 is then made into a specified island-shape to form a polycrystalline silicon layer 3 (Fig. 10(c)).

(4) An SiO_2 (silicon dioxide) layer having a thickness of 1000 Å, which later forms the gate insulating layer 4, is then formed on the glass substrate 2 such that the polycrystalline silicon layer 3 is covered (Fig. 10(d)).

(5) A metal layer 17 composed of aluminum, which later forms the gate electrode 5a, is then formed (Fig. 10(e)).

(6) The metal layer 17 is then patterned into a specified shape to form the gate electrode 5a (Fig. 10(f)).

(7) Impurity doping is then carried out using the gate electrode 5a as a mask (Fig. 10(g)). Specifically, doping is carried out by the ion doping method using phosphorus ions as the impurity. In this way, the channel region 3c located directly below the gate electrode 5a is not doped with impurities. Except for this channel region 3c of the polycrystalline silicon layer 3, the layer is doped with impurities. This doping is carried out at an acceleration voltage of 80 kV and a beam current density of 1 $\mu A/cm^2$ to fabricate n-type regions by high acceleration voltage.

(8) A photoresist 18 is then formed covering the gate electrode 5a (Fig. 10(h)).

(9) The photoresist 18 is then patterned by anisotropic etching to form a resist film 5b (Fig. 11 (i)). Here, the anistropic etching makes it possible to form the pattern of resist film 5b precisely.

(10) As shown in Fig. 11(j), the second impurity doping is then carried out using the resist film 5b as a mask. Specifically, doping is carried out by the ion doping method using phosphorus ions as the impurity. This doping is carried out at an acceleration voltage of 12 kV and a beam current density of 0.5 μA/cm^2 to fabricate high concentration n-type regions by low acceleration voltage.

(11) The interlayer insulating layer (SiOx) 6 is then formed (Fig. 11(k)).

(12) The contact holes 9a and 9b are then opened in the interlayer insulating layer 6 and the gate insulating layer 4 (Fig. 11(L)).

(13) Finally, the contact holes 9a and 9b are filled in with metal layers of, for example, Al by the sputtering method, and the upper portions of the metal layers are patterned into specified shapes to form the source electrode 7 and the drain electrode 8 (Fig. 11(m)). In this way, TFT 1 is produced.

In the foregoing example, although a method of producing an n-channel TFT was described, a p-channel TFT can be produced in the same way.

When light of 5000 cd/m^2 is applied from the rear surface of the thin film transistor fabricated by the production method described, the resulting OFF current is approximately 5 pA. As was stated earlier, during backlight irradiation, it is necessary that the OFF current be 10 pA or less.

Thus, the thin film transistor according to the present embodiment can ensure good display characteristics.

The voltage-current characteristics of thin film transistors are shown in Fig. 13, and the variation in OFF current within the area of the substrate is shown in Fig. 14. As shown in Fig. 13, the TFT 1 (graph L3) according to the present embodiment ensures a steady, large ON current and a small OFF current. As illustrated by Fig. 14, the TFT 1 fabricated in this way makes the variation in OFF current on the surface of the substrate minimal.

Fig. 15 shows the results of a simulation of the Vg-Id characteristics of a thin film transistor with the concentration of the n-type region as the parameter. When the sheet resistance of the LDD regions is 20 kΩ/□ or less, the OFF current suddenly increases. Therefore, it is necessary that the sheet resistance of the LDD regions be at least 20 kΩ/□ or higher. On the other hand, when the sheet resistance of the LDD regions is 100 kΩ/□ or higher, the ON current of the transistor diminishes and operation of the panel becomes unstable. Therefore, it is preferable that the sheet resistance of the LDD regions be within the range of 20 kΩ/□to 100 kΩ/□.

Generally, the backlight luminance is at the highest, approximately 5000 cd/m^2. In this case, in order to keep the photoconductive current to 10 pA or less, the depletion layer width Wd is obtained as follows. By substituting W=4, B=5000, and $I_{off}=10\times10^{-12}$ in the expression (10), a depletion layer width is obtained wherein Wd=0.4 μm.

Because the depletion layer width does not exceed the length of the LDD regions, by making the length ΔL of the LDD regions 0.4 μm or less, the depletion layer region is effectively 0.4 μm or less, making it possible to

realize a structure that suppresses (to 10 pA or less) photoconductive current. It should be noted that it is preferable that the LDD regions have a length greater than 0.1 μm as the electric field relaxation effect disappears when the length of the LDD regions is less than 0.1 μm, causing the OFF current to increase as is shown in Fig. 2(b).

In the expression (10), when the backlight luminance B is for example 2000 cd/m^2, the depletion layer width Wd is1 μm.

Therefore, because the depletion layer width does not exceed the length of the LDD regions, by making the length ΔL of the LDD regions 1.0 μm or less, the depletion layer region is effectively 1.0 μm or less, making it possible to suppress photoconductive current. It is even more preferable that the depletion layer width be 0.4 μm or less.

A device that is found, in an inspecting step, to have LDD regions with a length that exceeds 1.0 μm cannot meet the requirements for OFF characteristics. Therefore, by carrying out an inspecting step in which a TFT having LDD regions with a length ΔL of 1.0 μm or less is designated as a quality product, it is possible to distinguish quality products from inferior products and to eliminate the wasting of material in the production of panels.

As shown in Table 1, it was confirmed that with the TFTs of Examples 1 to 3 (those which satisfy the expression (2)), it is possible to suppress OFF current during irradiation of light, but with the TFTs of Examples 4 and 5 (those which do not satisfy the expression (6)), it is not possible to suppress OFF current during irradiation of light.

Table 1

	B (cd/m^2)	W (μm)	R (kΩ/□)	OFF current
Example 1	3000	4	50	good
Example 2	5000	2	50	good
Example 3	5000	3	30	good
Example 4	3000	4	80	bad
Example 5	5000	4	50	bad

In this way, by satisfying the relationship in the expression (6) between the new controlling factor (the sheet resistance of the drain region) and the channel width of the channel region, it is possible to regulate the range in which OFF current (photoconductive current) is suppressed during irradiation of light. Thus, by fabricating a thin film transistor that satisfies the relationship in the expression (6), OFF current can be suppressed, making it possible to provide a thin film transistor that can prevent crosstalk and luminance gradation and that realizes high performance efficient and high reliability.

Embodiment 1-2

A method of producing a thin film transistor in accordance to embodiment 1-2 of the present invention is described.

The thin film transistor according to the present embodiment 1-2 is such that LDD regions are formed to a short length of from 0.2 μm to 0.5 μm by anodic oxidation. As a result, the region on the drain side becomes a high concentration impurity region, and thus the depletion layer width does not spread beyond the length of the LDD region, making it possible to suppress photoconductive current. A specific description of the production

method is described as follows. Fig. 17(a) to 17(g) are schematic cross sectional views showing a method of producing a thin film transistor in accordance with embodiment 1-2 of the present invention, and Fig. 18(h) to 18(j) are schematic cross sectional views showing the same method of producing a thin film transistor.

In the same manner as embodiment 1-1, an a-Si layer 15 is deposited on a glass substrate 2, and melting and recrystallization (transformation into p-Si) is then carried out by laser annealing utilizing an excimer laser having a wavelength of 308 nm to form a polycrystalline silicon layer 16. The polycrystalline silicon layer 16 is then made into a specified island-shape to form a polycrystalline silicon layer 3. A gate insulating film 4 is then formed on the glass substrate 2 such that the polycrystalline silicon layer 3 is covered. (Figs. 17(a) to 17(d))

A metal layer 17 is then formed, a photoresist 17a formed in a pattern on the metal layer 17, and the metal film 17 patterned by an etching technique to form a gate electrode 5a. The side surfaces of the gate electrode 5a are then anodically oxidized to form oxide insulating layers 5b. (Fig. 17(f)).

As is shown in Fig. 17(g), impurity doping is then carried out using the gate electrode 5a as a mask. Specifically, doping is carried out by the ion doping method using phosphorus ions as the impurity. In this way, the channel region 3c located directly below the gate electrode 5a is not doped with impurities. In addition, in regions located directly below oxide insulating layers 5b and 5b, LDD regions 3d and 3e are formed and on the outer sides of these regions a channel region 3a and a drain region 3b are

formed.

As is shown in Fig. 18(h) to 18(j), an interlayer insulating layer (SiOx) 6 is then formed, contact holes 9a and 9b are opened in the interlayer insulating layer 6 and the gate insulating layer 4, and the contact holes 9a and 9b are filled in with metal layers of Al, for example, by a sputtering method, and the upper portions of the metal layers are patterned into specified shapes to form the source electrode 7 and the drain electrode 8. Thus, a TFT is fabricated.

The anodic oxidization carried out in the present embodiment makes it possible to form the LDD regions to a short length of from 0.2 μm to 0.5 μm. Because of this, the region on the drain side becomes a high concentration impurity region, and thus, the depletion layer width does not spread beyond the length of the LDD region. Therefore, it is made possible to suppress photoconductive current to a small value.

By this means, when the thin film transistor is OFF, a reduction in OFF current is realized because the low concentration impurity region becomes a high resistance layer that is drained of carriers. A guideline for the length of the LDD regions can be determined from the expression (2), eliminating the need to ensure a length for the LDD regions more than is necessary for the reduction of OFF current. By satisfying the expression (6) in addition to the expression (2), when the transistor is on, electrons that serve as carriers gather in the low concentration impurity regions under the gate electrode in response to the electric field of the gate electrode, making a low resistance region, and a reduction in ON current does not occur. Thus, thin film transistors that satisfy both the expression (2) and the expression

(6) make it possible to hold OFF current to a small value while ensuring sufficient ON current.

Additionally, by employing for the impurity doping a low acceleration ion doping method carried out at an acceleration voltage in the range of from 10 kV to 30 kV and a beam current density in the range of from 0.5 $\mu A/cm^2$ to 1 $\mu A/cm^2$, damage caused during doping is reduced because the acceleration voltage of the ions is low during the ion doping. Furthermore, in cases where a resist is used as a mask during the impurity doping, the resist is not altered and may be easily removed.

Embodiment 1-3

The present embodiment 1-3 is described with reference to Figs. 19 to 22.

Fig. 19 is a plan view showing the wiring pattern of a C-MOS inverter that utilizes thin film transistors in accordance with embodiment 1-3 of the present invention, Fig. 20 is a diagram of the equivalent circuit of the C-MOS inverter, and Fig. 21 is a cross sectional view of Fig. 19 taken along line X-X'.

A C-MOS inverter 50 is comprised in a driver circuit of, for example, a liquid crystal display device. This C-MOS inverter 50 comprises an n-channel TFT 22 and a p-channel TFT 23. The n-channel TFT 22 has the same construction as that of the n-channel TFT 1 of embodiment 1, and like parts are accorded like reference numerals.

The p-channel TFT 23 is a conventional TFT without an LDD structure. More specifically, the TFT 23 is constructed such that a polycrystalline silicon layer 24, a gate insulating layer 4 composed of SiO_2 (silicon dioxide),

a gate electrode 25 composed of aluminum, and an interlayer insulating layer 6 composed of SiO_2 are deposited in that order on a glass substrate 2. The polycrystalline silicon layer 24 comprises a channel region 24c located directly below the gate electrode 25, a source region 24a (p+ layer), and a drain region 24b (p+ layer), the source region 24a and the drain region 24b being disposed on either side of a channel region 24c. A source electrode 26 and a drain electrode 27 composed of, for example, aluminum are provided in the TFT 23. The source electrode 26 is connected to the source region 24a via a contact hole 28a formed in the gate insulating layer 4 and the interlayer insulating layer 6. The drain electrode 27 is connected to the drain region 24b via a contact hole 28b formed in the gate insulating 4 and the interlayer insulating layer 6. The gate electrode 5 of the n-channel TFT 22 and the gate electrode 25 of the p-channel TFT 23 are commonly connected to an input terminal 30 as is shown in Fig. 20. The drain electrode 8 of the n-channel TFT 22 and the drain electrode 27 of the p-channel TFT 23 are commonly connected to an output terminal 31 as is shown in Fig. 19.

In the present embodiment 1-3, only the drain side of the n-channel TFT has the LDD structure described in embodiment 1-1. Thus, it is made possible to reduce the size of the TFT, to keep the distance between the source and drain to approximately 6 μm, and to reduce size by about 50% in comparison with TFTs having an LDD region formed on either side of the source and drain, thereby realizing the miniaturization of TFTs.

It should be noted that both the n-channel TFT and the p-channel TFT may have an LDD structure. However, in cases in which only one of the

n-channel TFT and the p-channel TFT has an LDD structure in order to keep the area of the array substrate occupied by the circuit to a small area, it is preferable that the n-channel TFT have the LDD structure. This is due to the fact that in a comparison of the respective motilities of holes, which serve as the carriers in the p-channel TFT, and electrons, which serve as the carriers in an n-channel TFT, the mobility of electrons is significantly higher. Therefore, when the same electric field is applied to a p-channel TFT and an n-channel TFT, because impact to the n-channel TFT by the carriers is greater, the n-channel TFT is more easily degraded. Thus, from the standpoint of improving reliability in the preventing of degradation of a TFT, it is preferable that the n-channel TFT have the LDD structure.

The points of operation of a C-MOS inverter during on/off when an n-channel transistor is biased are shown in Fig. 22. In the n-channel TFT of such an inverter, the gate electrode is operated by a voltage having a polarity with respect to the current source on the negative side such that the voltage is always higher than 0 V. Therefore, the current source on the negative side always functions as the source electrode of the n-channel TFT and the output side always functions as the drain electrode. For this reason, employing a circuit in which this portion is such that only the output side portion has the construction described above contributes to a reduction in the area of the array substrate occupied by a portion of the circuit. It also contributes to a reduction in parasitic capacitance.

Supplementary Remarks

Although in embodiments 1-1 to 1-3, LDD regions having one variety of concentration were described, the present invention is not limited to this.

Rather, a plurality of LDD regions having differing concentrations may be provided. Namely, constructing the LDD regions of a plurality of junction regions having impurity concentrations that gradually decrease in the direction of the channel region makes it possible to change impurity concentration at multiple levels and thus to further relax concentration of an electric field in the semiconductor layer.

It is possible that an LDD region be formed only between the drain region and the channel region whereby it is made possible to reduce the area of the thin film transistor while still realizing the advantageous effects of a reduction in OFF current and the like.

The embodiments 1-1 to 1-3 were described using top-gate TFTs, but the present invention may also be applied to bottom-gate TFTs.

Thin film transistors described in embodiments 1-1 to 1-3 may be applied to EL devices in addition to liquid crystal display devices. In other words, a plurality of the thin film transistors of embodiments 1-1 to 1-3 serving as switching elements are formed on a substrate, and by providing an EL device with this substrate, a structure that suppresses photoconductive current is realized.

Second Invention Group

General Concepts of the second invention group

An object of the present embodiment is to hold the length of LDD regions to a necessary minimum and to suppress a reduction in ON current while also suppressing the OFF current of the thin film transistor (hereinafter referred to as "TFT"), thereby realizing a TFT having high performance and high reliability. In consideration of this, in order to

determine the truly necessary length for the LDD regions, the present inventors carried out operation analysis by simulations and determined how much the region exposed to an electric field extends.

Fig. 23(a) to 23(d) are graphs showing the results of a simulation of Vg-Id characteristics when the length of an LDD region, the sheet resistance being the parameter, is changed from 0.5 μm to 3 μm.

From these results, it was confirmed that Vg-Id characteristics are highly dependant on the concentration of the LDD region and not on the length of the LDD region. In the following, the reason for this is examined.

Fig. 24(a) and 24(b) show the results of a simulation of an electric field in a channel region and an LDD region when a TFT is in the OFF state (Vg=−10V and Vd=6V).

From the simulation results, it was confirmed that the length of the region exposed to an electric field is dependant on sheet resistance. When the sheet resistance is 20 kΩ/□, the length of the region is approximately 0.4 μm and when the sheet resistance is 100 kΩ/□, the length of the region is approximately 1.0 μm.

Therefore, it was discovered that even if the LDD region is made larger than the region exposed to an electric field, there is no advantageous effects in terms of the electric field relaxation effect, but rather, it is only that the resistance is inserted in serial in the channel region of the transistor.

Fig. 25(a) and 25(b) are graphs showing the relationship between the length (ΔL) of an LDD region and OFF current and the relationship between the length (ΔL) of an LDD region and ON current in an actual TFT having an LDD region. It should be noted that the sheet resistance of the LDD

region is 100 kΩ/□.

As is shown in Fig. 25a, even if the LDD region is made longer than 1.0 μm, there is no further reduction in OFF current, as is reflected by the results of the simulation. In addition, as is shown in Fig. 25(b), when the LDD region is made longer than 1.5 μm, ON current is reduced without being sufficiently ensured. According to these results, setting the length of the LDD region to the range of from 1 μm to 1.5 μm makes it possible to hold the OFF current to a small value while ensuring a sufficient ON current. In the following embodiments, TFTs fabricated according to the simulations are specifically described. In the actual fabrication process of a TFT, in order to be certain that LDD regions like that described above are obtained, mask alignment may be determined using alignment marks as is described later.

Embodiment 2-1

Fig. 26 is a simplified cross sectional view of a thin film transistor in accordance with embodiment 2-1 of the present invention, and Fig. 27 is a schematic plan view of Fig. 26.

In the present embodiment 2-1, an example of the present invention being applied to an n-channel thin film transistor is given. This thin film transistor (hereinafter referred to as "TFT") 101 is constructed such that a polycrystalline silicon layer 103 having a thickness of 500 Å, a gate insulating layer 104 composed of SiO_2 (silicon dioxide) and having a thickness of 1000 Å, a gate electrode 105 composed of aluminum, and an interlayer insulating layer 106 composed of SiO_2 are deposited in that order on a glass substrate 102. The gate electrode 105a is formed with a resist

film 105b formed thereon. It should be noted that a metal film may be used instead of the resist film 105b.

The polycrystalline silicon layer 103 comprises a channel region 103c located directly below the gate electrode 105a, a source region 103a (n+ layer) having a high impurity concentration, a drain region (n+ layer) 103b having a high impurity concentration, and low concentration impurity regions (LDD regions: n− layers) 103d and 103e having low impurity concentrations. The low concentration impurity region 103d is interposed between the source region 103a and the channel region 103c, and the low concentration impurity region 103e is interposed between the drain region 103b and the channel region 103c. These low concentration impurity regions 103d and 103e are located directly below portions 105b1 and 105b2 of the resist film 105b, which portions 105b1 and 105b2 protrude from the gate electrode 105a. Therefore, the junction interface between the low concentration impurity region 103d and the source region 103a is substantially aligned with an end surface of the resist film 105b (the left side end surface in Fig. 1), and the junction interface of the low concentration impurity region 103d and the channel region 103c is substantially aligned with an end surface of the gate electrode 105a (the left side end surface of Fig. 1). Likewise, the junction interface between the low concentration impurity region 103e and the drain region 103b is substantially aligned with an end surface of the resist film 105b (the right side end surface in Fig. 1), and the junction interface of the low concentration impurity region 103d and the channel region 103c is substantially aligned with the end surface of the gate electrode 105a (the

right side end surface of Fig. 1). In the present embodiment, the length ΔL of the low concentration impurity region is set within the range of from 1 μm to 1.5 μm and the channel width W to 5 μm.

In the TFT 101, a source electrode 107 and a drain electrode 108 composed of, for example, aluminum are provided. The source electrode 107 is connected to the source region 103a via a contact hole 109a formed in the gate insulating layer 104 and the interlayer insulating layer 106. The drain electrode 108 is connected to the drain region 103b via a contact hole 109b formed in the gate insulating layer 104 and the interlayer insulating layer 106.

A method of producing a thin film transistor in accordance with embodiment 2-1 of the present invention is now described. Fig. 28(a) to 28(h) and Fig. 29(a) to (e) are schematic cross sectional views showing a method of producing a thin film transistor in accordance with embodiment 2-1 of the present invention, and Fig. 30 is a flow chart showing a method of producing a thin film transistor in accordance with embodiment 2-1 of the present invention.

(1) First, an a-Si layer 105 having a film thickness of 500 Å is deposited on the glass substrate 102 by plasma CVD, and dehydrogenation is carried out at 400°C (Fig. 28(a)). The purpose of this dehydrogenation is to prevent ablation of the Si film by the desorption of hydrogen when crystallization is carried out. For the step of forming the a-Si, in addition to plasma CVD, it is also possible to utilize processes such as reduced pressure CVD and sputtering. Moreover, by utilizing these methods such as the plasma CVD method, a polysilicon film can be directly deposited on the substrate. In

these cases, the need for a laser-annealing step discussed later is eliminated.

(2) The melting and recrystallization (transformation into p-Si) of the a-Si layer 115 is then carried out by laser annealing utilizing an excimer laser having a wavelength of 308 nm to form a polycrystalline silicon layer 116 (Fig. 28(b)).

(3) The polycrystalline silicon layer 116 is then made into a specified island-shape to form a polycrystalline silicon layer 103 (Fig. 28(c)).

(4) A SiO_2 (silicon dioxide) layer having a thickness of 1000 Å, which later forms the gate insulating layer 104, is then formed on the glass substrate 102 such that the polycrystalline silicon layer 103 is covered (Fig. 28(d)).

(5) A metal layer 117 composed of aluminum, which later forms the gate electrode 105a, is then formed (Fig. 28(e)).

(6) The metal layer 117 is then patterned into a specified shape to form the gate electrode 105a (Fig. 28(f)).

(7) A first impurity doping is then carried out using the gate electrode 105a as a mask (Fig. 28(g)). Specifically, the doping is carried out by the ion doping method using phosphorus ions as the impurity. In this way, the channel region 103c located directly below the gate electrode 105a is not doped with impurities, and the regions A and B of the polycrystalline silicon layer 103 not including the channel region 103c are doped with impurities to become an n− layer. This doping is carried out at an acceleration voltage of 80 kV and a beam current density of 1 $\mu A/cm^2$ to fabricate low concentration n− type regions by high acceleration voltage.

(8) A photoresist 118 is then formed covering the gate electrode 105a (Fig. 28(h)).

(9) The photoresist 118 is then patterned to form a resist film 105b (Fig. 29(a)). The process of step (9) is now described in detail using Fig. 31 to 34. Fig. 31(a) to 31(d) are schematic cross sectional process diagrams illustrating the process of forming LDD regions, Fig. 32 a perspective view of the photomask and the substrate, Fig. 33(a) and 33(b) are plan views of the same, and Fig. 34(a) and 34(b) are schematic cross-sectional views of the thin film transistor after the formation of LDD regions.

As shown in Fig. 7, a photomask 140 and the substrate 102 are disposed so as to be opposed to one other. A light source for aligning (not shown in the figure) is disposed in position above the photomask 140, and aligning is carried out by applying a laser beam from the light source for aligning to alignment marks 141 and 142 formed on each of the photomask 140 and the substrate 102.

In specified positions on the photomask 140 (102 positions in the corners of the photomask) the alignment marks 141, which are substantially square-shaped, are formed. In a central position of the photomask 140, the pattern (not shown in the figure) of a masking film to be transferred to the substrate 102 is formed.

On the glass substrate 102, in positions corresponding to those of the alignment marks 141, the alignment marks 142 are formed. The alignment marks 142 are substantially square-shaped, transparent regions that are enclosed by black regions. Though not shown in the figure, the alignment marks 141 and 142 are not limited to a square shape, but may

have, for example, a circular shape.

As is shown in Fig. 33(a), when the photomask 140 and the substrate 102 are not misaligned, the alignment marks 141 formed on the photomask 140 are aligned with the centers of the transparent regions of the alignment marks 142 formed on the substrate 102. When LDD regions are formed under these conditions, the length ΔL of the LDD regions 103d and 103e is set to 1.25 μm.

Supposing the substrate 102 and the photomask 140 are misaligned and the alignment marks 141 do not fit into the alignment marks 142, it is understood that the length of the LDD regions formed becomes longer than 1.5 μm, and thus in such cases, the substrate and the photomask are fixed so as to be aligned with the alignment marks 141 in the center of the alignment marks 142. Even if the alignment marks 141 are arranged so as to be in the center of the alignment marks 142, in practice, as is shown in Fig. 33 (b), there are cases of shifting in the horizontal direction in terms of space. However, in the present invention, because the accuracy of the alignment device is ± 0.25 μm, it is possible to carry out alignment so that the alignment marks 41 are positioned within the alignment marks 42. In such a way, as is shown in Fig. 34(a) and 34(b), the length of the LDD regions 3d and 3e formed can be kept within the range of from 1 μm to 1.5 μm. It should be noted that while the accuracy of the alignment device is ± 0.25 μm, supposing an alignment device having even better accuracy is used, variations in the LDD regions can be further reduced.

The process of aligning the substrate and the photmask is now described.

As is shown in Fig. 31(a), a photoresist to become a masking film is formed on the gate electrode 105a.

As is shown in Figs. 31(b) and 31(c), the photoresist is exposed through the photomask and developed to form a masking film 105b to a specified pattern.

In this case, as has been discussed, exposure is carried out after it has been confirmed that the alignment marks 141 fit into the transparent portions of the alignment marks 142.

(10) As shown in Fig. 29(b), the second impurity doping is then carried out using the resist film 105b as a mask. Specifically, the doping is carried out by the ion doping method using phosphorus ions as the impurity. This doping is carried out at an acceleration voltage of 12 kV and a beam current density of 0.5 $\mu A/cm^2$ to fabricate high concentration n-type regions by low acceleration voltage.

By this means, regions of the polycrystalline silicon layer 103 not including a region located directly below the resist film 105b are doped with ions. Thus, regions not covered by the resist film 105b within the regions A and B that have already been doped with impurities in the first ion doping (corresponding to source region 103a and drain region 103b) are doped again with impurities to become high concentration impurity regions (n+ layers). On the other hand, regions covered by the resist film 105b within the regions A and B (corresponding to low concentration impurity regions 103d and 103e) are not doped with impurities at the time of the second ion doping and thus become low concentration impurity regions (n− layers). In this way, the low concentration impurity region 103d (n− layer) is formed

between the source region 103a (n+ layer) and the channel region 103c, and the low concentration impurity region 103e (n− layer) is formed between the drain region 103b (n+ layer) and the channel region 103c. Moreover, because the first ion doping is carried out using the gate electrode 105a as a mask and the second ion doping is carried out using the resist film 5b as a mask, the source region 103a, the low concentration impurity regions 103d and 103e, and the drain region 103b are formed so as to be self aligned to one another, and the overlapping portions of the gate electrode 5 and the source region 103a and that of the gate electrode 105 and the drain region 103b are held to a short length to the extent that they do not need to be taken into account. Thus, it is made possible to form a thin film transistor having LDD regions with a length in the range of from 1 μm to 1.5 μm and to suppress, to as small a value as possible, reduction in ON current while holding OFF current to a small value.

(11) The interlayer insulating layer (SiOx) 106 is then formed (Fig. 29(c)).

(12) The contact holes 109a and 109b are then opened in the interlayer insulating layer 106 and the gate insulating layer 104 (Fig. 29(d)).

(13) Finally, the contact holes 109a and 109b are filled in with metal layers of Al, for example, by the sputtering method, and the upper portions of the metal layers are patterned into specified shapes to form the source electrode 107 and the drain electrode 108 (Fig. 29(e)). In this way, TFT 101 is fabricated.

In the foregoing example, a method of producing an n-channel TFT was described, however, a p-channel TFT can be produced in the same way.

Fig. 35 is a graph showing the current/voltage characteristics of a thin film transistor produced by the method described above. Fig. 36 is a graph showing the variation in OFF current within the area of a substrate.

As is shown in Fig. 35, a TFT 101 (graph of L3) in accordance with the present embodiment 2-1 ensures a stable, large ON current and a small OFF current because the LDD regions, which are high resistance regions, have a short length in the range of from 1 μm to 1.5 μm.

It is of course possible to make the length of the LDD regions even smaller by improving the alignment accuracy of the aligner. In addition, when the carrier concentration of the n− regions is increased, the region exposed to an electric field gets smaller, but because at the same time the peak value of the electric field increases, the OFF current increases.

Fig. 37 is a graph showing a simulation of the Vg-Id characteristics of a thin film transistor, the concentration of the LDD regions being the parameter.

When the sheet resistance of the LDD regions is 20 kΩ/□, the OFF current suddenly increases. Therefore, it is necessary that the sheet resistance of the n-regions be a value at least 20 kΩ/□ or higher. On the other hand, when the sheet resistance of the LDD regions is 100 kΩ/□ or higher, the ON current of a transistor is reduced and the operation of the panel becomes unstable. Therefore, it is preferable that the sheet resistance of the LDD regions be in the range of from 20 kΩ/□ to 100 kΩ/□.

By employing for the first impurity doping a low acceleration ion doping method carried out at an acceleration voltage in the range of from 10 kV to 30 kV and a beam current density in the range of from 0.5 μA/cm^2 to 1

μA/cm^2, damage caused during doping is reduced because the acceleration voltage of the ions is low during the ion doping.

In cases where a resist is used as a mask during the first impurity doping, the resist is not altered and may be easily removed.

As for the second impurity doping, by employing a high acceleration ion doping method carried out at an acceleration voltage of 30 kV or higher and a beam current density of 1 μA/cm^2 or higher makes it possible to implant a sufficient number of ions in the polysilicon at the time of the second ion doping.

In the present embodiment 2-1, the length ΔL of the LDD regions in the TFT 101 are set in the range of from 1 μm to 1.5 μm, and operation is carried out under the conditions of a source-drain voltage Vlc of 6V and a channel width W of 6 μm. However, because OFF current is generally determined by the electric field between the source and drain and the Vlc is only applied to the channel region/LDD regions, the strength of the electric field is represented by Vlc/ΔL (Solid State Electron, 38, 2075 (1995)). The strength of the electric field is represented by the following expression.

$$4\times10^6 < Vlc/\Delta L < 6\times10^6$$

In addition, because the OFF current is proportional to the channel width W, the relationship between the length ΔL of the LDD regions, the source-drain voltage Vlc, and the channel width W can be expressed by the expression (3) below.

(3)

$$\Delta L > (W \cdot Vlc)/36$$

The meaning of the expression (3) is now explained. In cases the size

of a TFT has been reduced, the values for ΔL and W become smaller, and along with this, the source-drain voltage Vlc decreases. In consideration of this, the characteristics of TFTs in which the length ΔL of the LDD regions, the source-drain electrode Vlc, and the channel width V have been varied are shown in Table 2.

Table 2

	Vlc (V)	ΔL (μm)	Vlc/ΔL	W (μm)	W·Vlc/36	3·(W/L)	ON current	OFF current
Example 1	6	1	$6 \cdot 10^6$	5	0.83	1.25	good	good
Example 2	6	1.5	$4 \cdot 10^6$	5	0.83	1.25	bad	good
Example 3	3	0.5	$6 \cdot 10^6$	5	0.41	1.25	good	good
Example 4	3	0.75	$4 \cdot 10^6$	3	0.25	0.75	good	good
Example 5	6	2	$3 \cdot 10^6$	5	0.83	1.25	bad	good
Example 6	6	0.5	$12 \cdot 10^6$	5	0.83	1.25	good	bad
Example 7	3	1	$3 \cdot 10^6$	3	0.25	0.75	bad	good

(L=12 μm, ON current good: ON current is ensured, OFF current good: OFF current is suppressed)

As shown in Table 2, OFF current could be suppressed in Examples 1 to 5 and 7 (those that satisfy expression (1)), but OFF current could not be suppressed in Example 6 (one that does not satisfy expression (3)).

In addition, the relationship between the length ΔL of the LDD regions, the channel width L of the channel region, and the channel width W of the channel region is represented by expression (4') below:

$$\Delta L < 3 \cdot (W / L) \tag{4'}$$

where W is the channel width of the channel region.

The expression (4) illustrates the limits of ON current, the conditions being derived from the fact that ON current is proportional to W/L. The conditions of ON current are derived from the experimental results in which

ON current is reduced, where W/L=0.5 and ΔL is 1.5μm or less. As shown in Table 1, Examples 1,3, 4, and 6, in which expression (4) is satisfied, ensure the ON current.

As for conditions desirable for ensuring ON current to a greater degree than is achieved by expression (4'), it is possible to ensure ON current by employing the expression (4) below.

(4)

$$\Delta L < 1.5 \cdot (W / L)$$

Thus, when a thin film transistor is OFF, a reduction in OFF current is realized because the low concentration impurity region becomes a high resistance layer that is drained of carriers. In addition, a guideline for the length of the LDD regions can be determined from the expression (3), eliminating the need to ensure a length for the LDD region more than is necessary to reduce OFF current. By satisfying the expression (4) in addition to the expression (3), when the transistor is on, electrons that serve as carriers gather in the low concentration impurity regions under the gate electrode and a reduction in ON current does not occur. Thus, thin film transistors that satisfy both the expression (3) and the expression (4) make it possible to hold OFF current to a small value while ensuring sufficient ON current.

It should be noted that operation was carried out at a channel width of 5 μm, but that in cases in which the channel width W of the channel region is miniaturized to 2 μm or less, the relational expressions (3) and (4) are particularly effective guidelines in the fabricating of a thin film transistor.

Embodiment 2-2

The present embodiment 2-2 is such that in the production process of embodiment 2-1, without employing alignment marks to obtain LDD regions having a length in the range of from 1 μm to 1.5 μm in the case of forming a resist film 105b, a thin film transistor having LDD regions with a length within the range described can be obtained by including an inspecting step of designating a TFT that satisfies the condition of having a length of LDD regions in the range of from 1 μm to 1.5 μm a quality product. Therefore, while sufficiently ensuring ON current, it is possible to hold OFF current to a small value. It should be noted that, in the present embodiment 2-2, the LDD regions are not limited to those having a length in the range of from 1 μm to 1.5 μm, but may be set within the range determined by expressions (3) and (4) described in embodiment 2-1.

Supplementary Remarks

Although in embodiments 2-1 to 2-2, low concentration impurity regions having one level of concentration were described, the present in invention is not limited to this. Rather, a plurality of low concentration impurity regions having differing concentrations may be provided. Namely, constructing the lightly doped region of a plurality of junction regions having impurity concentrations that gradually decrease in the direction of the channel region makes it possible to change impurity concentration at multiple levels and thus to further relax concentration of an electric field in the semiconductor layer.

It is possible that the low concentration impurity region be formed only between the drain region and the channel region whereby it is made

possible to reduce the area of the thin film transistor while still realizing the advantageous effects of a reduction in OFF current and the like. Moreover, such a thin film transistor may have applications other than a liquid crystal display device.

In the case of a C-MOS inverter circuit, which has a p-channel thin film transistor and an n-channel thin film transistor, at least the n-channel thin film transistor may be constituted by a thin film transistor in accordance to embodiment 2-1 or 2-2.

INDUSTRIAL APPLICABILITY

As is explained above, by employing the constructions of the present invention, the problems to be solved by the present invention are sufficiently overcome.

Specifically, by the first invention group, while sufficiently ensuring ON current, it is made possible to hold photoconductive current to a small value during light irradiation. In addition, power consumption is reduced, and advantageous effects with respect to improvement in reliability and TFT characteristics are considerable.

By the second invention group, it is possible to provide a thin film transistor that while sufficiently ensuring ON current, makes it possible to hold OFF current to a small value, and with which, power consumption is reduced and advantageous effects with respect to improvement in reliability and TFT characteristics are considerable.

What is claimed is:

1. A thin film transistor comprising:

a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, and a drain region, the source region and the drain region disposed on either side of the channel region;

wherein a depletion layer is formed between the channel region and the drain region; and

the width of the depletion layer and photoconductive current are in a proportional relationship, the photoconductive current generated when the channel region is irradiated with light, and the width of the depletion layer is equal to or less than a value obtained on the basis of the proportional relationship so that the photoconductive current falls within a range of specified permissible values.

2. A thin film transistor according to claim 1, wherein the relationship of expression (1)

(1)

$$(R+30)\cdot W < A$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region and W (μm) is the channel width of the channel region.

3. A thin film transistor according to claim 2, wherein the relationship of expression (2)

(2)

$$(R+30)\cdot W<1\times10^{3}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region and W (μm) is the channel width of the channel region.

4. A thin film transistor according to claim 3, wherein the channel width W of the channel region is 2 μm or less.

5. A thin film transistor according to claim 3, wherein the sheet resistance of the drain region is in the range of from 20 kΩ/□ to 100 kΩ/□.

6. A thin film transistor according to claim 4, wherein the sheet resistance of the drain region in the range of from 20 kΩ/□ to 100 kΩ/□.

7. A thin film transistor for use as a switching element of a liquid crystal display device, the thin film transistor comprising a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, and a drain region, the source region and the drain region disposed on either side of the channel region, wherein:

a low concentration impurity region having an impurity concentration less than that of the source region and the drain region is formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, and the length ΔL of the low concentration impurity region is 1.0 μm or less, the luminance of a backlight of the liquid crystal display device being 2000 (cd/m^2) or higher.

8. A thin film transistor comprising a polycrystalline silicon semiconductor layer having formed therein a channel region, a source region, a drain region, and a low concentration impurity region having an impurity concentration less than that of the source region and the drain region, the source region and the drain region being disposed on either side of the channel region and the low concentration impurity region being formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region, the thin film transistor wherein:

the relationship of expression (3)

(3)

$$\Delta L > (W \cdot Vlc)/36$$

is satisfied, where ΔL (μm) is the length of the low concentration impurity region, Vlc (V) is the source-drain voltage, and W (μm) is the channel width of the channel region.

9. A thin film transistor according to claim 8, wherein the relationship of expression (4)

(4)

$$\Delta L < 1.5 \cdot (W / L)$$

is satisfied, where L (μm) is the channel length of the channel region.

10. A thin film transistor according to claim 9, wherein the channel width W (μm) of the channel region is 2 μm or less.

11. A thin film transistor according to claim 9, wherein the sheet

resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.

12. A thin film transistor according to claim 10, wherein the sheet resistance of the low concentration impurity region is in the range of from 20 kΩ/□ to 100 kΩ/□.

13. A thin film transistor according to claim 11, wherein the low concentration impurity region is formed only in the region between the drain region and the channel region.

14. A liquid crystal display device comprising:

a liquid crystal panel portion comprising thin film transistors serving as switching elements, each of the thin film transistors being a thin film transistor of claim 1; and

a backlight portion for supplying light from a rear surface side of the liquid crystal panel portion;

wherein the relationship of expression (5)

(5)

$$(R+30)\cdot B\cdot W < C$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the luminance of the backlight portion, and W (μm) is the channel width of the channel region.

15. A liquid crystal display device according to claim 14, wherein the relationship of expression (6)

(6)

$$(R+30)\cdot B\cdot W<1\times10^{6}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the luminance of the backlight portion, and W (μm) is the channel width of the channel region.

16. An EL display device comprising a light-emitting layer and a counter electrode formed thereon, the light-emitting layer being on a pixel electrode upper layer formed on a substrate having thin film transistors, the display device wherein:

each of the thin film transistors is a thin film transistor of claim 1, and

the relationship of expression (5)

(5)

$$(R+30)\cdot B\cdot W<C$$

is satisfied, where B (cd/m^2) is the light intensity of light applied to a channel region of each of the thin film transistors.

17. An EL display device according to claim 16, wherein the relationship of the expression (6)

(6)

$$(R+30)\cdot B\cdot W<1\times10^{6}$$

is satisfied, where R (kΩ/□) is the sheet resistance of the drain region, B (cd/m^2) is the light intensity of light applied to the channel region, and W (μm) is the channel width of the channel region.

18. A method of producing a thin film transistor, comprising the steps

of:

forming a polycrystalline silicon semiconductor layer on an insulating substrate;

forming a gate insulating film on the polycrystalline silicon semiconductor layer;

forming a gate electrode in a pattern on the gate insulating film;

carrying out anodic oxidation by oxidizing a side surface of the gate electrode to form a metal oxide film covering the side surface of the gate electrode; and

doping the polycrystalline silicon semiconductor layer with impurities, the gate electrode being used as a mask;

wherein the thickness of the metal oxide film formed in the step of carrying out anodic oxidation is controlled to make the length ΔL of a low concentration impurity region formed in the step of carrying out impurity doping 1.0 μm or less.

19. A method of producing a thin film transistor, comprising the steps of:

forming a polycrystalline silicon semiconductor layer on an insulating substrate;

forming a gate insulating film on the polycrystalline silicon semiconductor layer;

forming a gate electrode in a pattern on the gate insulating film;

carrying out a first impurity doping by doping the polycrystalline silicon semiconductor layer with impurities, using the gate

electrode as a mask;

forming a masking film on a semiconductor region doped with impurities in the step of carrying out a first impurity doping, the masking film being formed in a pattern by anisotropic etching;

carrying out a second impurity doping by doping the polycrystalline silicon semiconductor layer with impurities using the masking film as a mask so that an impurity concentration difference exists between a region under the masking film and regions other than the region under the masking film, whereby a low concentration impurity region having an impurity concentration lower than that of the source region and the drain region is formed in at least one of a region between the source region and the channel region and a region between the drain region and the channel region and by making the length of the low concentration impurity region 1.0 μm or less.

20. A method of producing a thin film transistor according to claim 19, further comprising a step of inspecting by designating the thin film transistor having a low concentration impurity region with a length ΔL of 1.0 μm or less a quality product.

Fig. 1

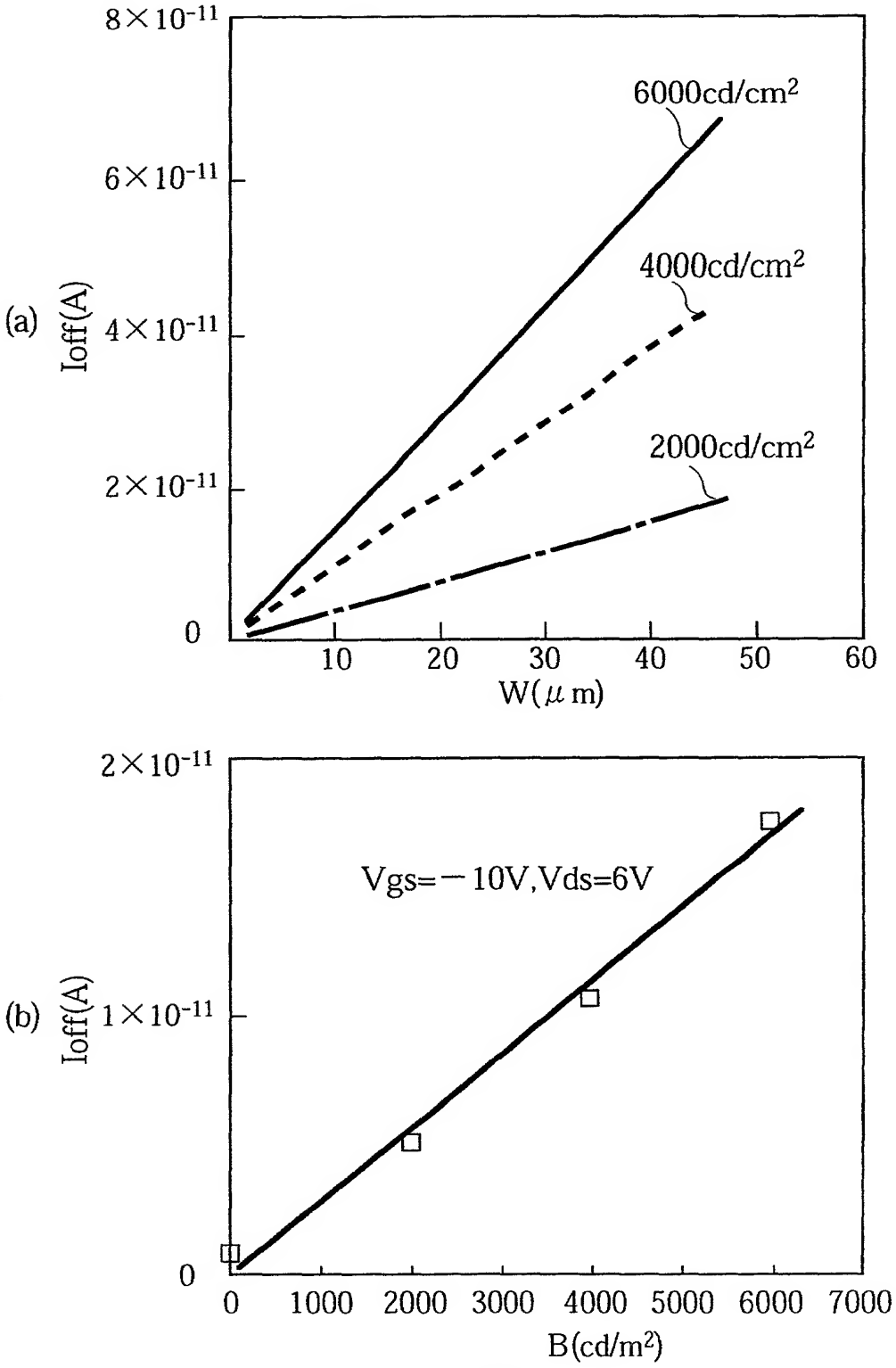

(a)
Ioff(A)
8×10-11
6×10-11
4×10-11
2×10-11
0
6000cd/cm2
4000cd/cm2
2000cd/cm2
10
20
30
40
50
60
W(μm)
(b)
Ioff(A)
2×10-11
1×10-11
0
Vgs=−10V,Vds=6V
0
1000
2000
3000
4000
5000
6000
7000
B(cd/m2)

Fig. 2

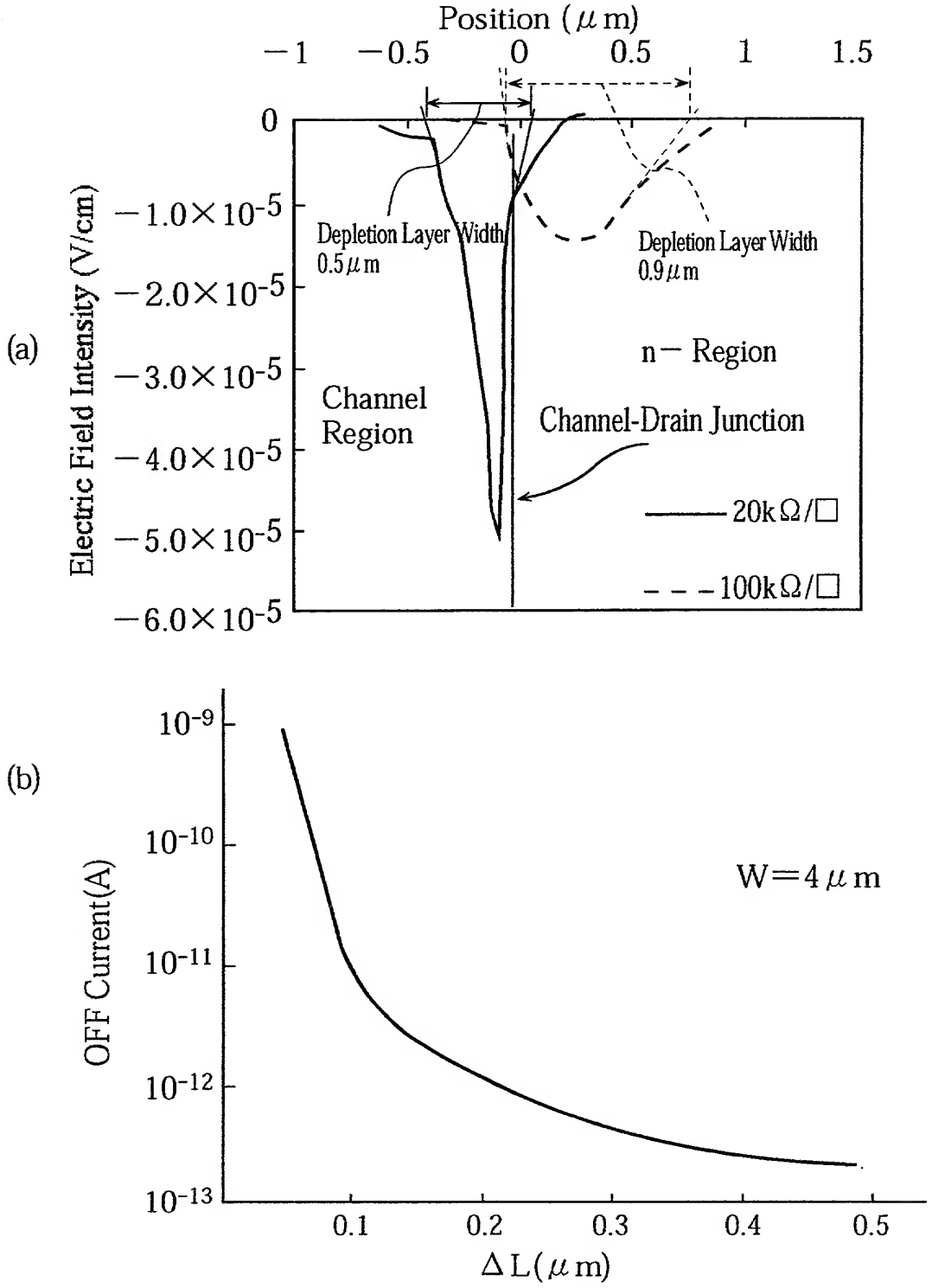

(a)
Position (μm)
−1
−0.5
0
0.5
1
1.5
0
−1.0×10-5
−2.0×10-5
−3.0×10-5
−4.0×10-5
−5.0×10-5
−6.0×10-5
Electric Field Intensity (V/cm)
Depletion Layer Width
0.5μm
Depletion Layer Width
0.9μm
n− Region
Channel
Region
Channel-Drain Junction
20kΩ/□
100kΩ/□
(b)
10-9
10-10
10-11
10-12
10-13
OFF Current(A)
W=4μm
0.1
0.2
0.3
0.4
0.5
ΔL(μm)

Fig. 3

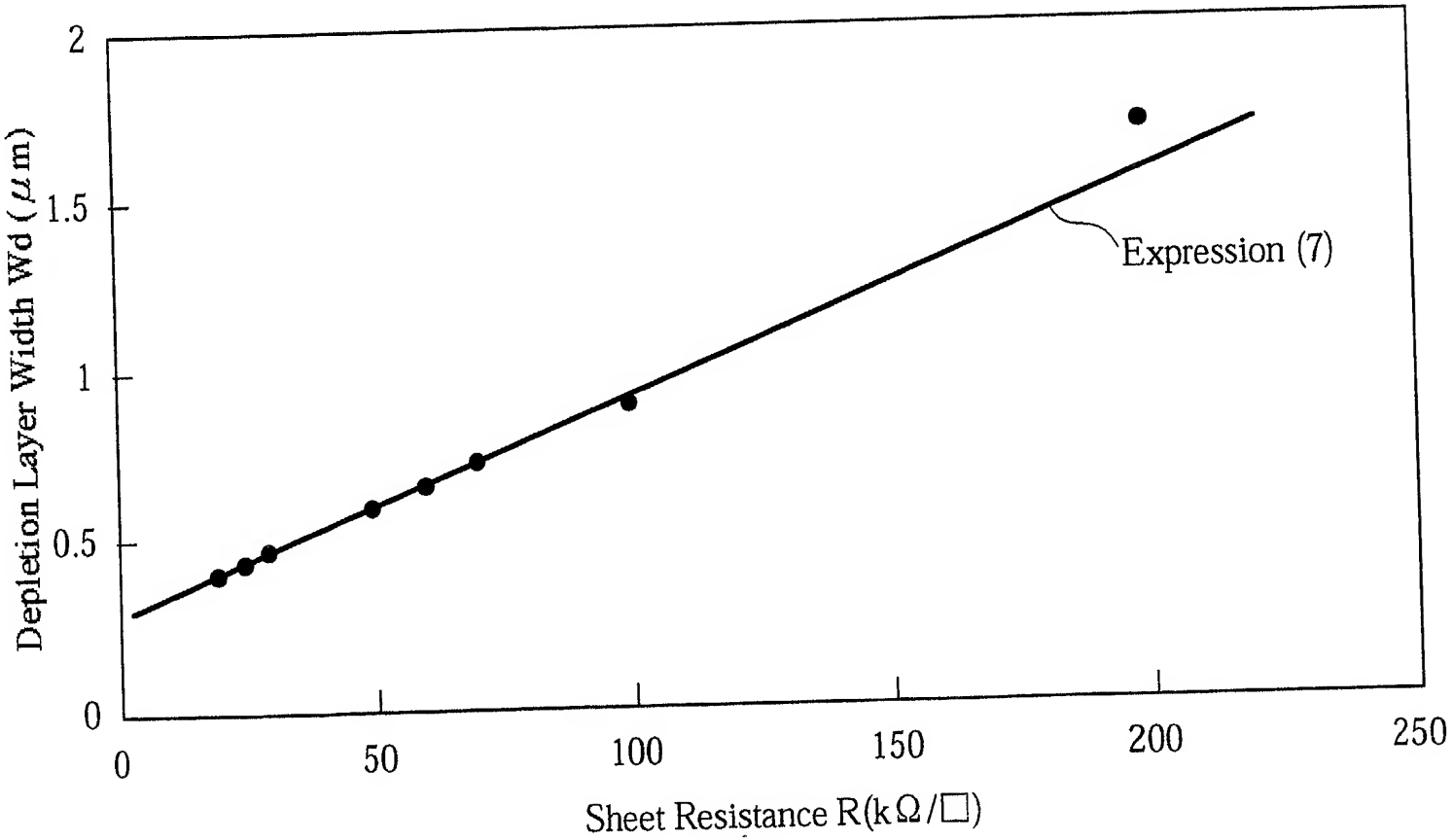


Fig. 4

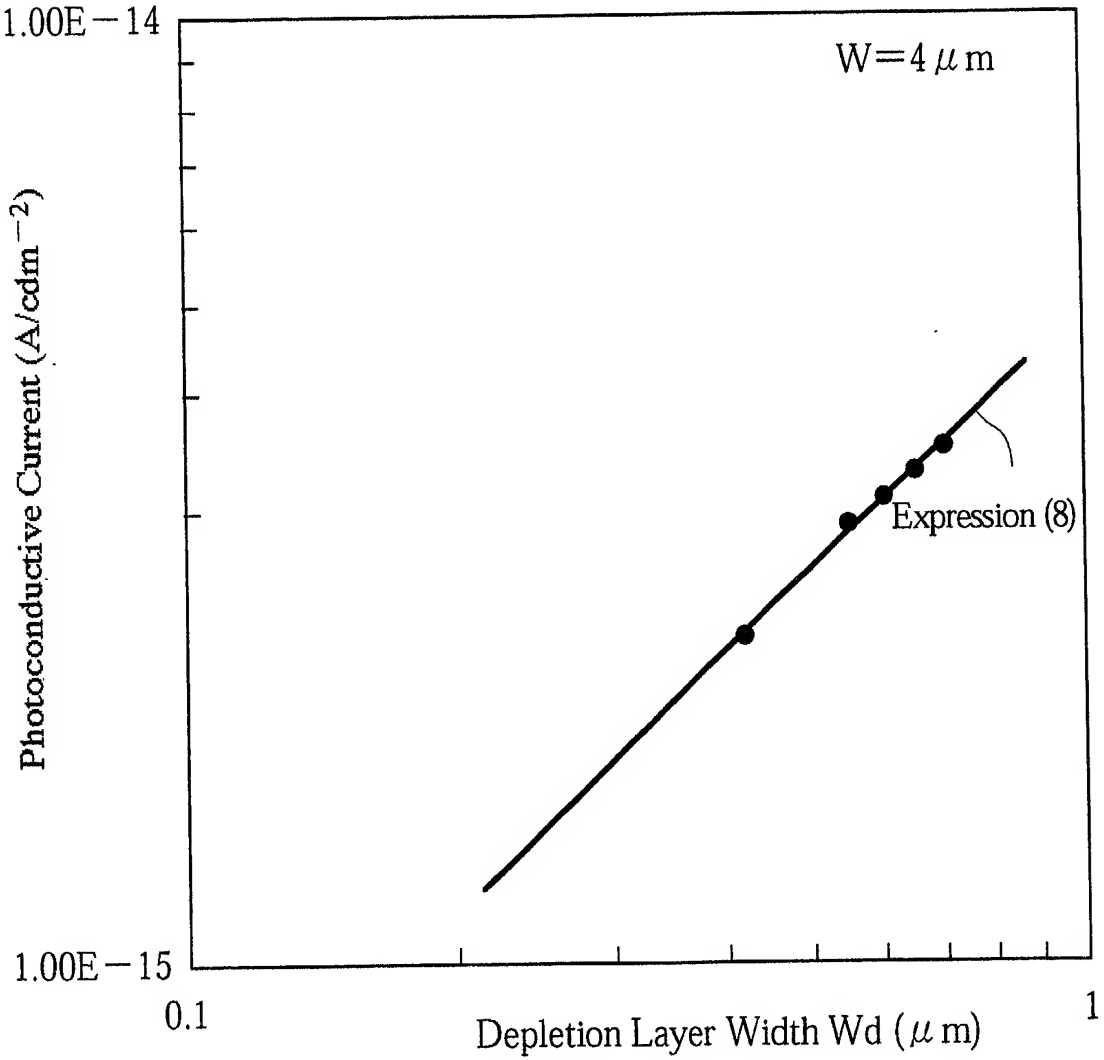
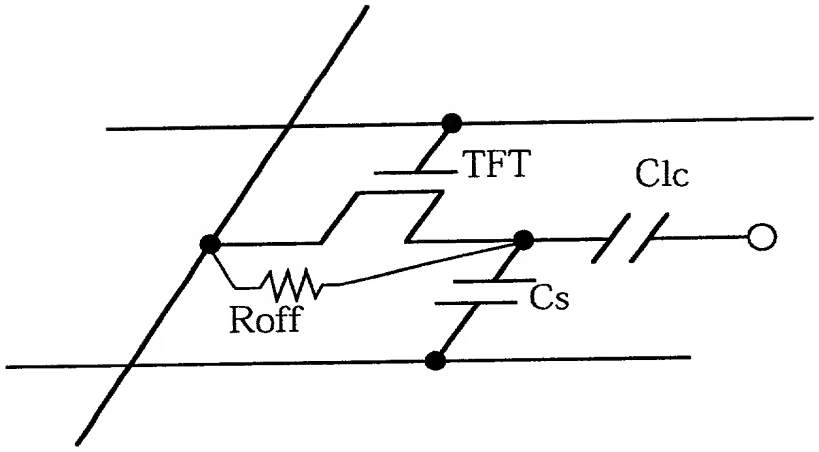
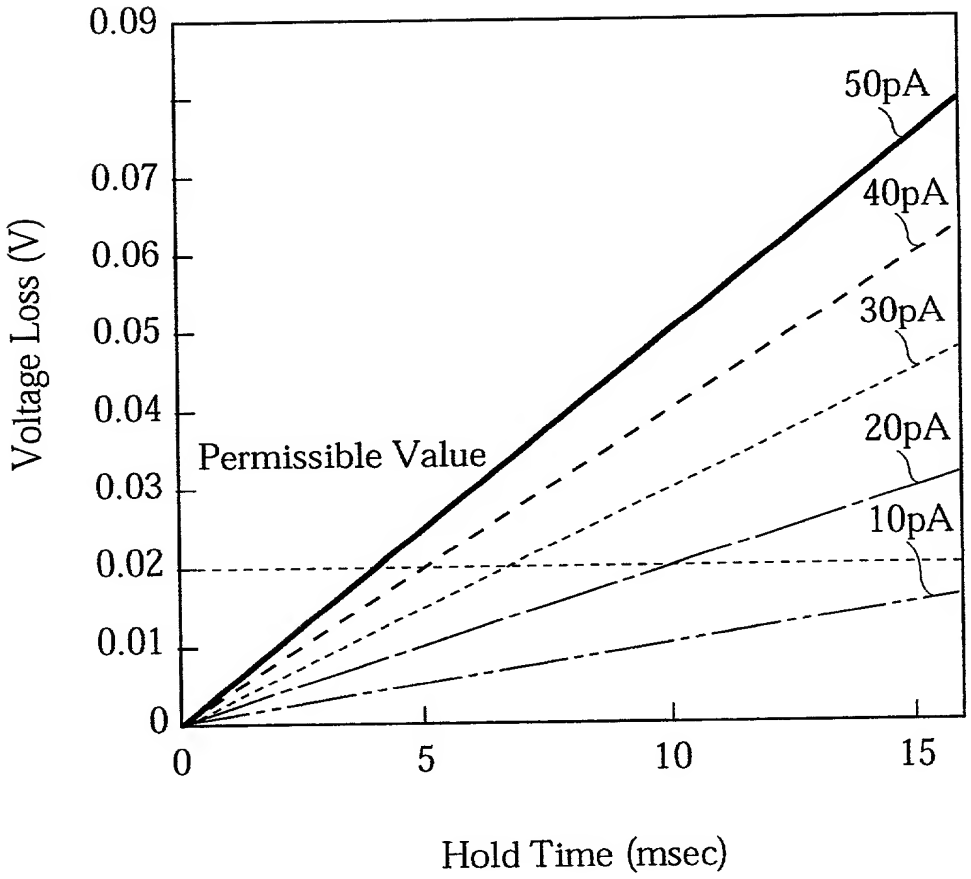


Fig. 5



Roff (Off Resistance of TFT) = Vsd/Ioff
Ioff: Off Current of Transistor
Vsd: Source-Drain Voltage
Cs: Storage Capacitor
Clc: Liquid Crystal Capacitor

Fig. 6


0.09
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
Voltage Loss (V)
Permissible Value
50pA
40pA
30pA
20pA
10pA
0
5
10
15
Hold Time (msec)

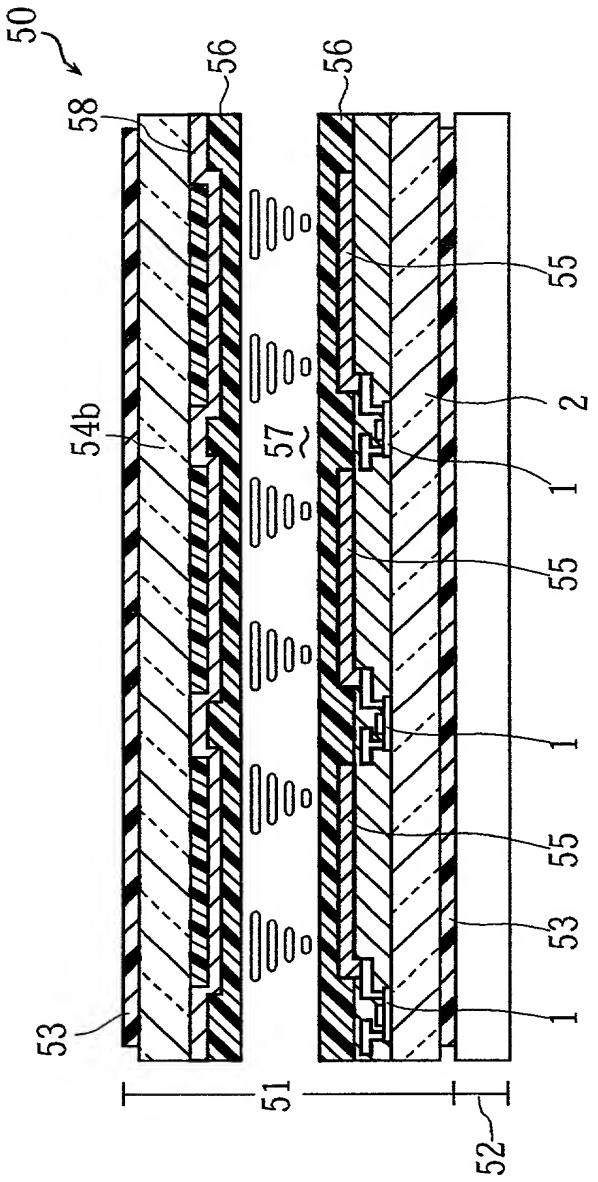


Fig. 7

Fig. 8

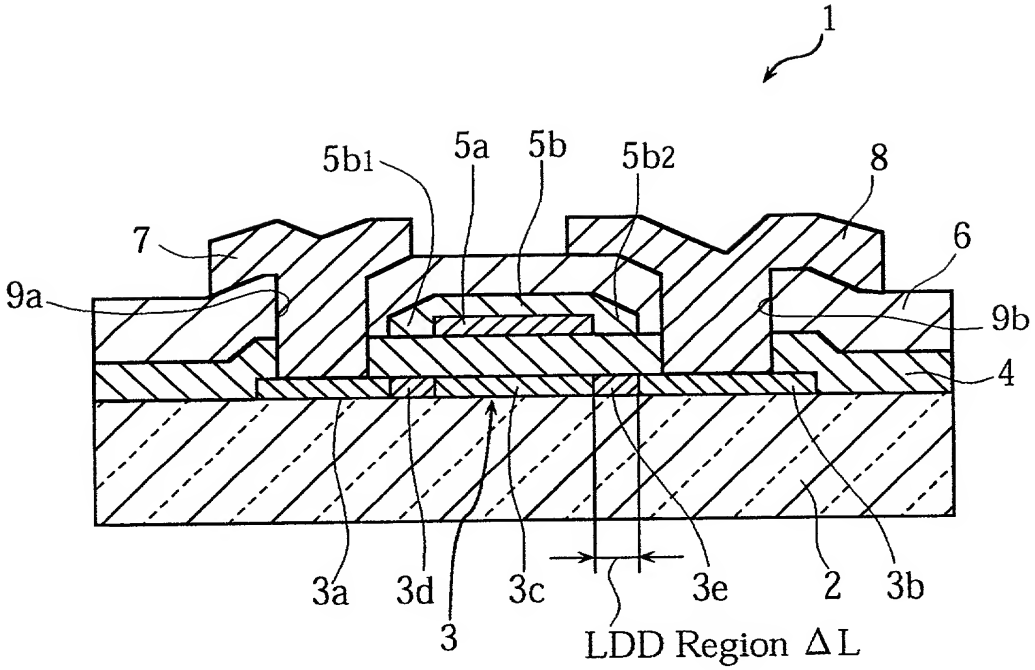


Fig. 9

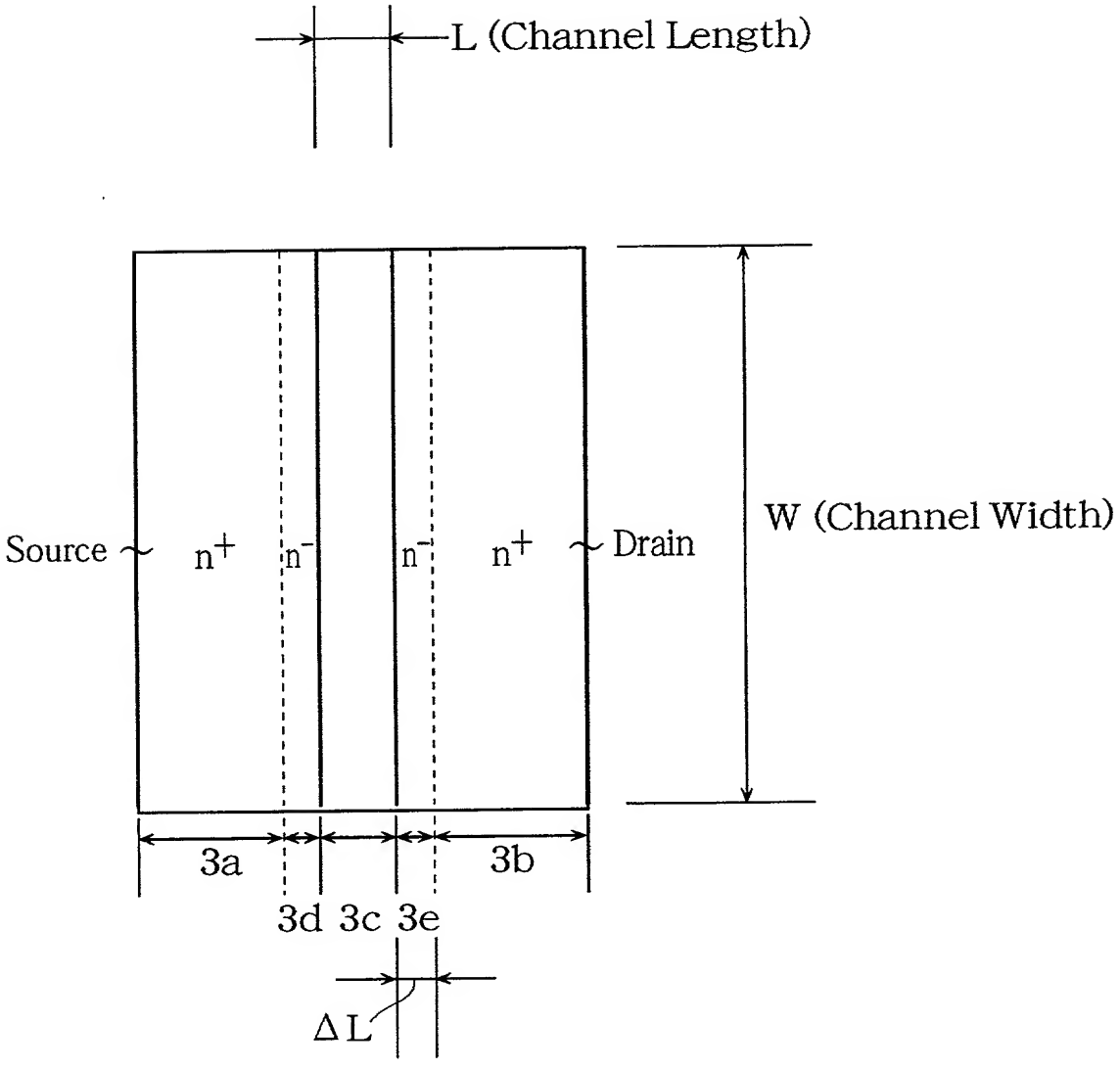

L (Channel Length)
Source
n+
n-
n-
n+
Drain
W (Channel Width)
3a
3b
3d 3c 3e
ΔL

Fig. 10

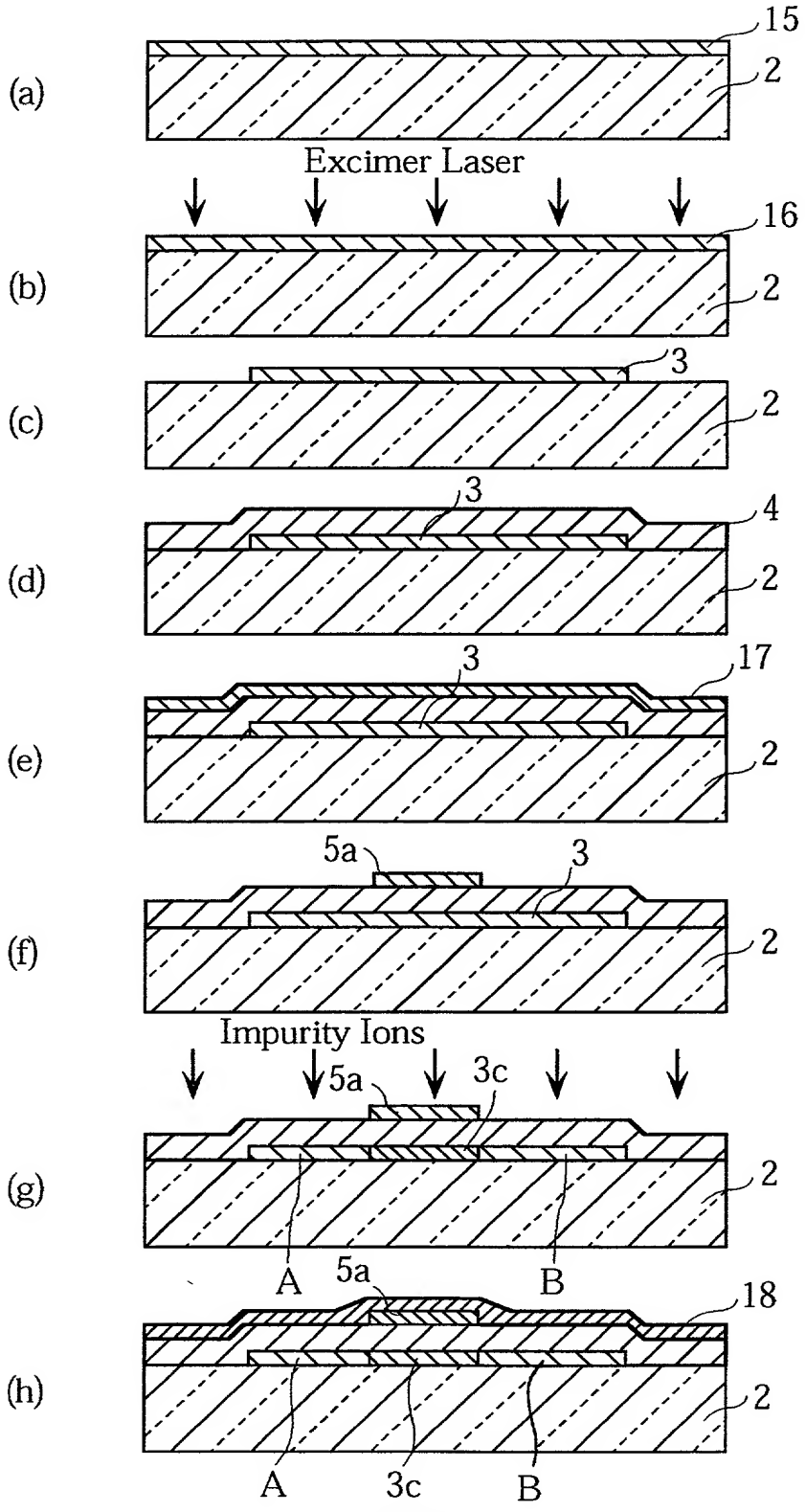

(a)
15
2
Excimer Laser
(b)
16
2
(c)
3
2
(d)
3
4
2
(e)
3
17
2
(f)
5a
3
2
Impurity Ions
(g)
5a
3c
2
A
5a
B
(h)
18
2
A
3c
B

Fig. 11

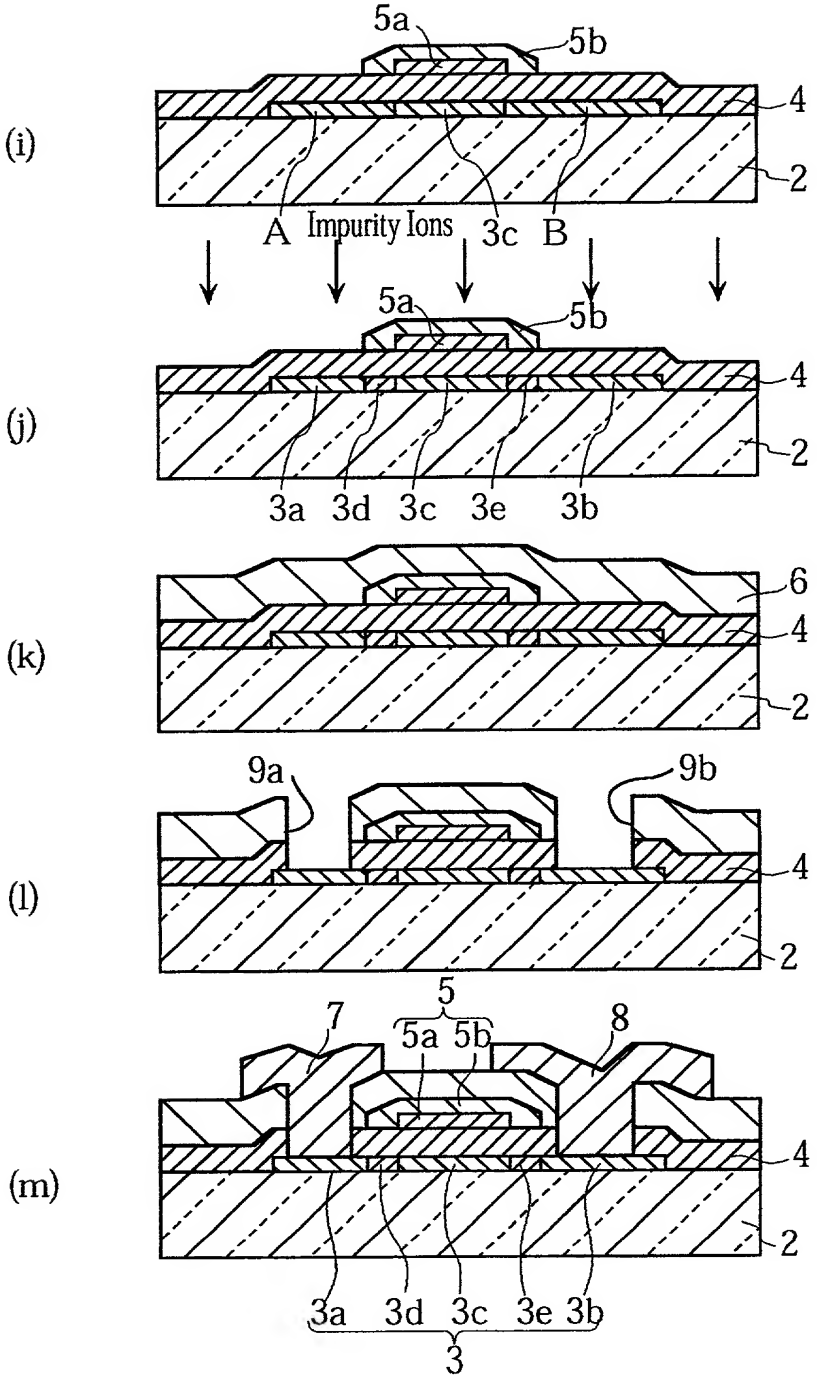

(i)
5a
5b
4
2
A
Impurity Ions
3c
B
(j)
5a
5b
4
2
3a
3d
3c
3e
3b
(k)
6
4
2
(l)
9a
9b
4
2
5
7
5a
5b
8
(m)
4
2
3a
3d
3c
3e
3b
3

Fig. 12

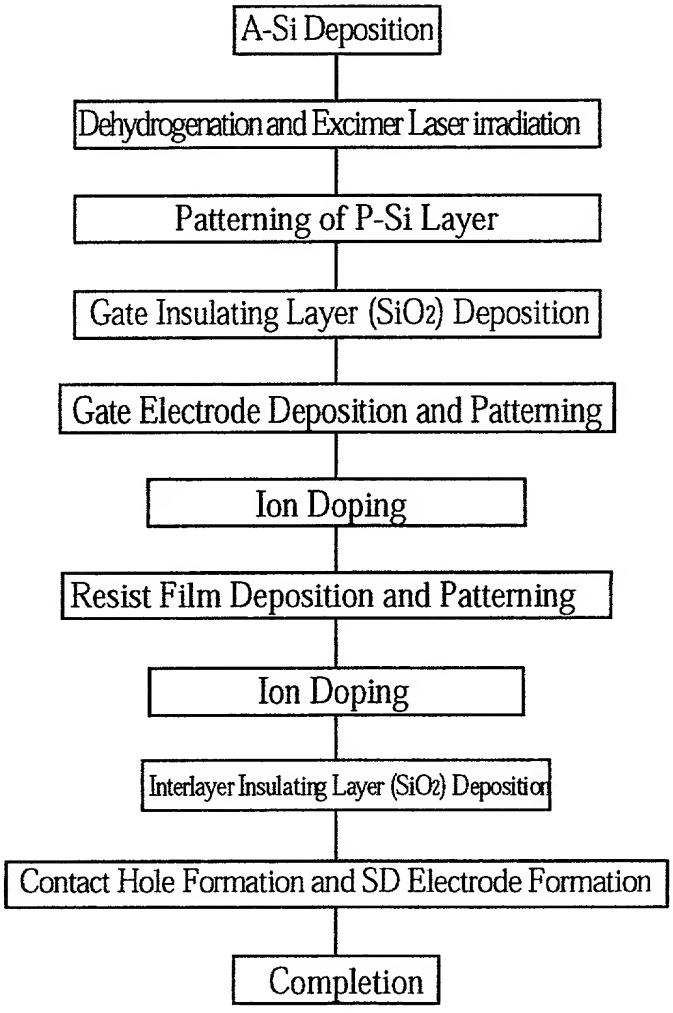

A-Si Deposition
Dehydrogenation and Excimer Laser irradiation
Patterning of P-Si Layer
Gate Insulating Layer (SiO2) Deposition
Gate Electrode Deposition and Patterning
Ion Doping
Resist Film Deposition and Patterning
Ion Doping
Interlayer Insulating Layer (SiO2) Deposition
Contact Hole Formation and SD Electrode Formation
Completion

Fig. 13

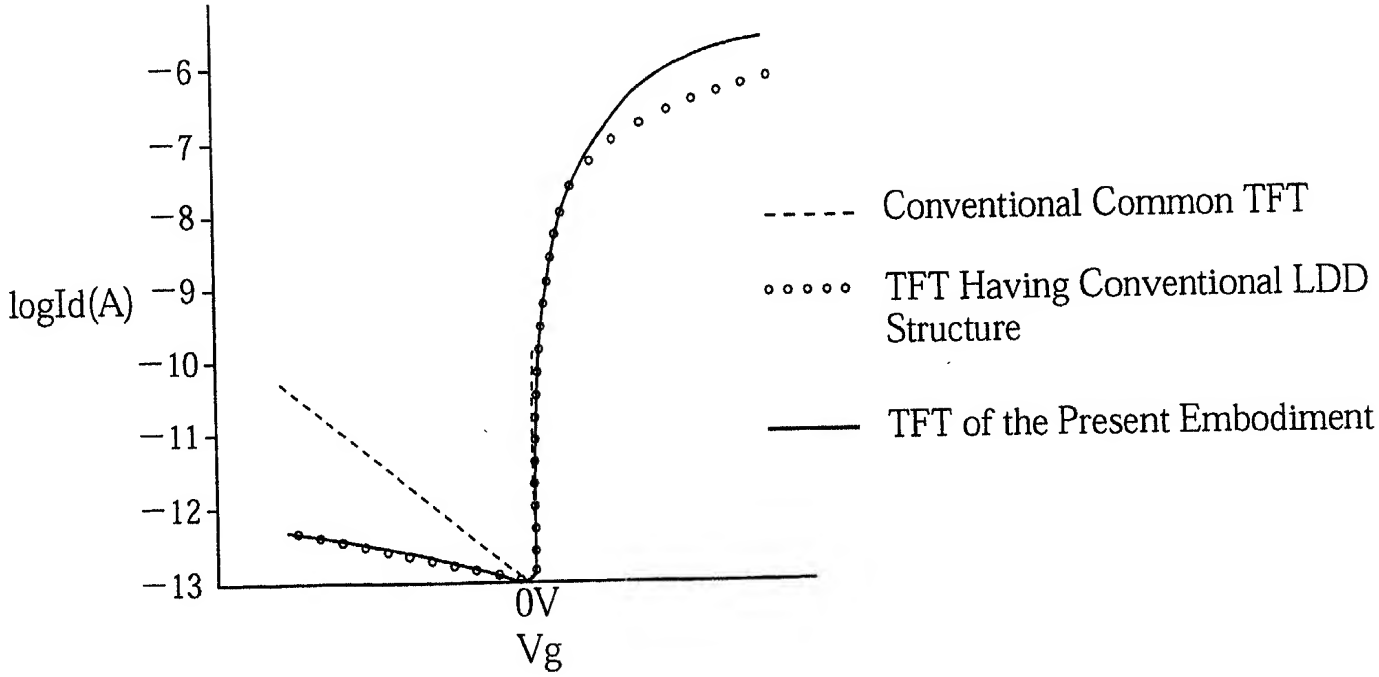


Fig. 14

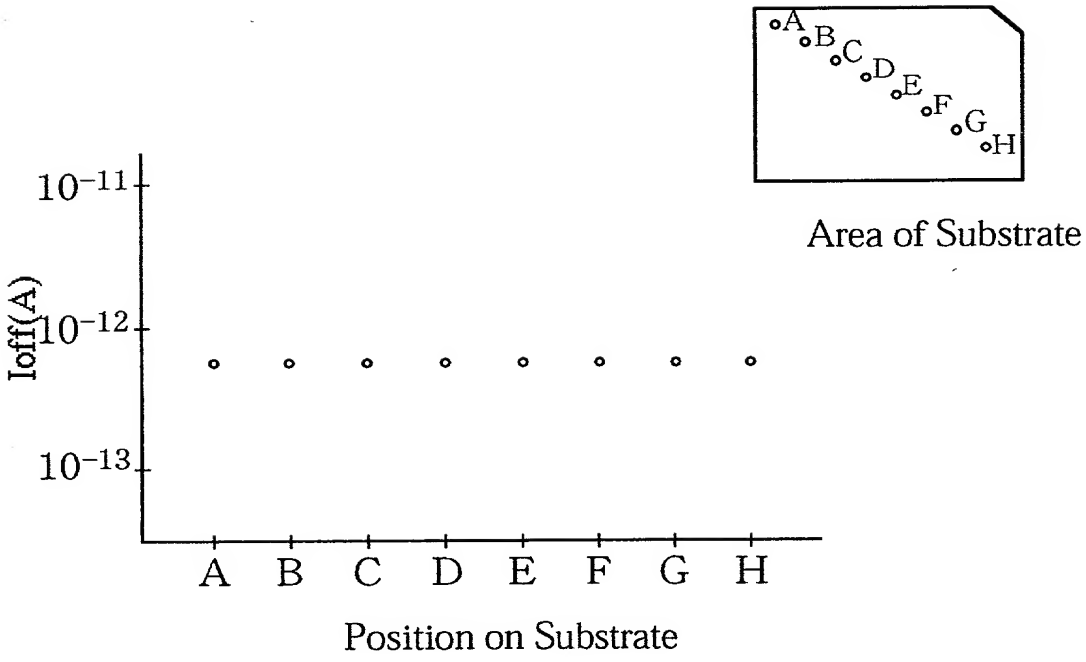

A
B
C
D
E
F
G
H
Area of Substrate
10^{-11}
10^{-12}
10^{-13}
Ioff(A)
A B C D E F G H
Position on Substrate

Fig. 15

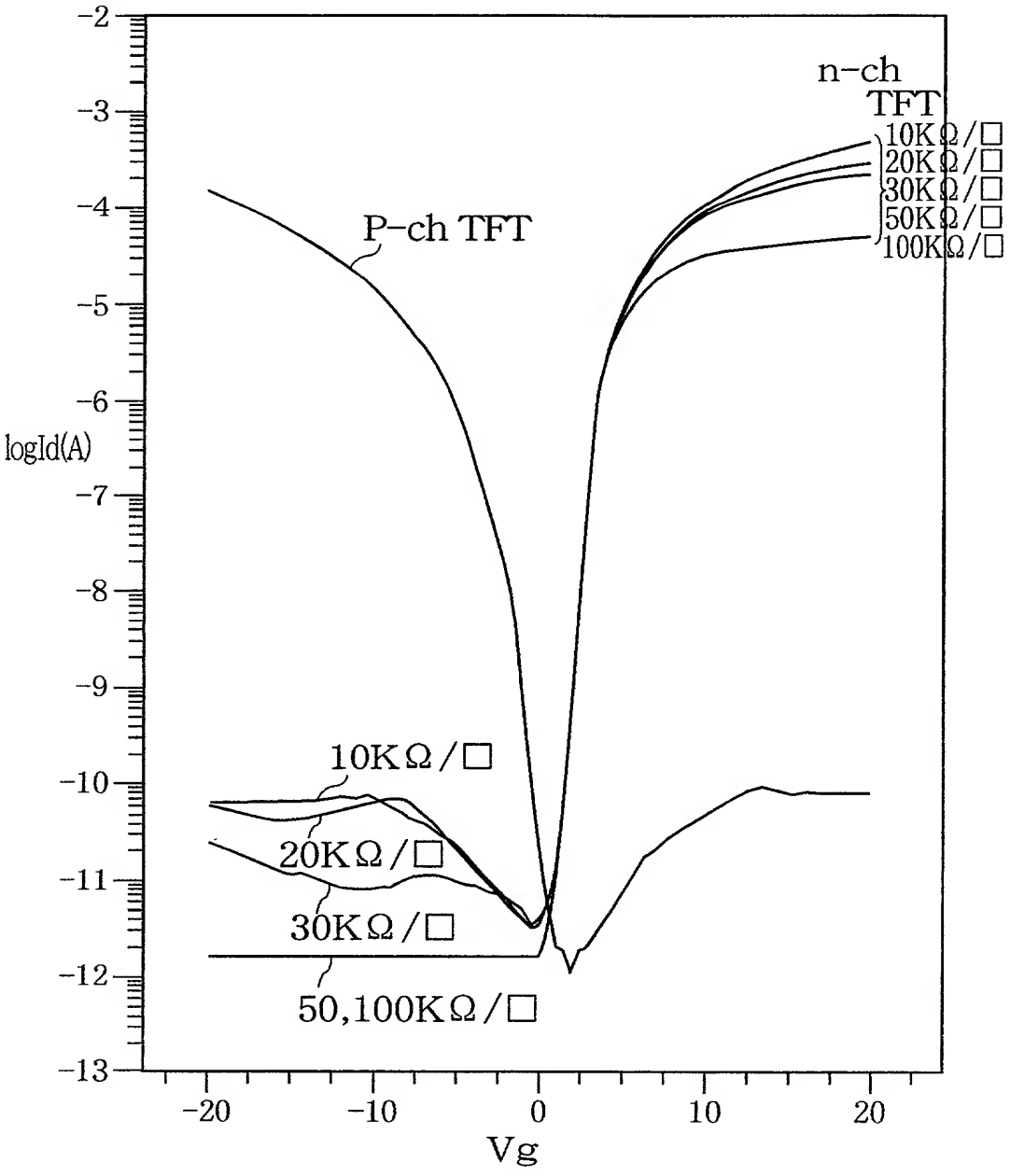

n-ch
TFT
10KΩ/□
20KΩ/□
30KΩ/□
50KΩ/□
100KΩ/□
P-ch TFT
logId(A)
10KΩ/□
20KΩ/□
30KΩ/□
50,100KΩ/□
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-20
-10
0
10
20
Vg

Fig. 16

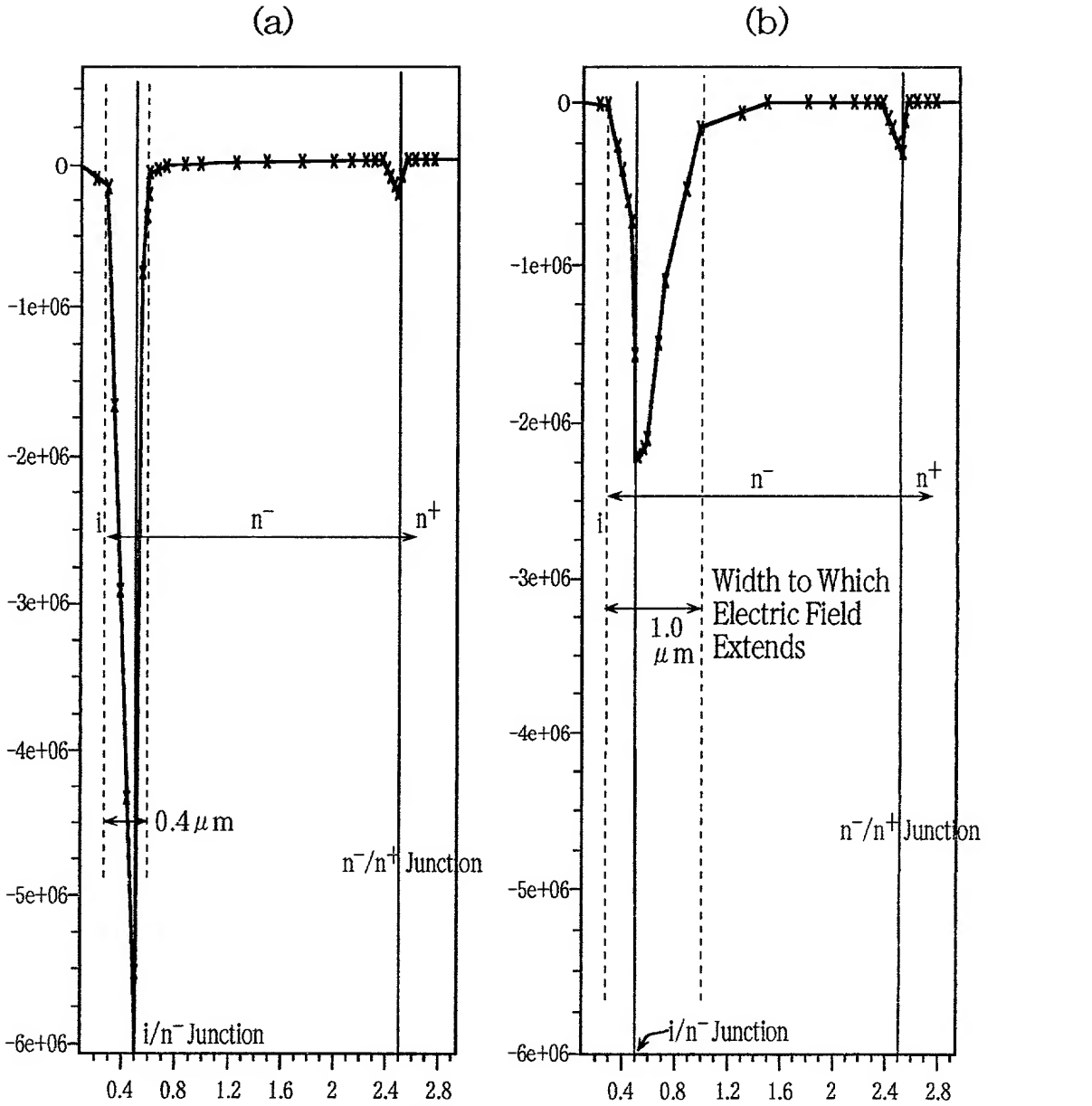

(a)
(b)
0
-1e+06
-2e+06
-3e+06
-4e+06
-5e+06
-6e+06
i
n⁻
n⁺
0.4 μm
n⁻/n⁺ Junction
i/n⁻ Junction
Width to Which Electric Field Extends
1.0 μm
0.4 0.8 1.2 1.6 2 2.4 2.8
n⁻ Sheet Resistance 20kΩ/□
n⁻ Sheet Resistance 100kΩ/□
Vg = −10V Vd = 6V

Fig. 17

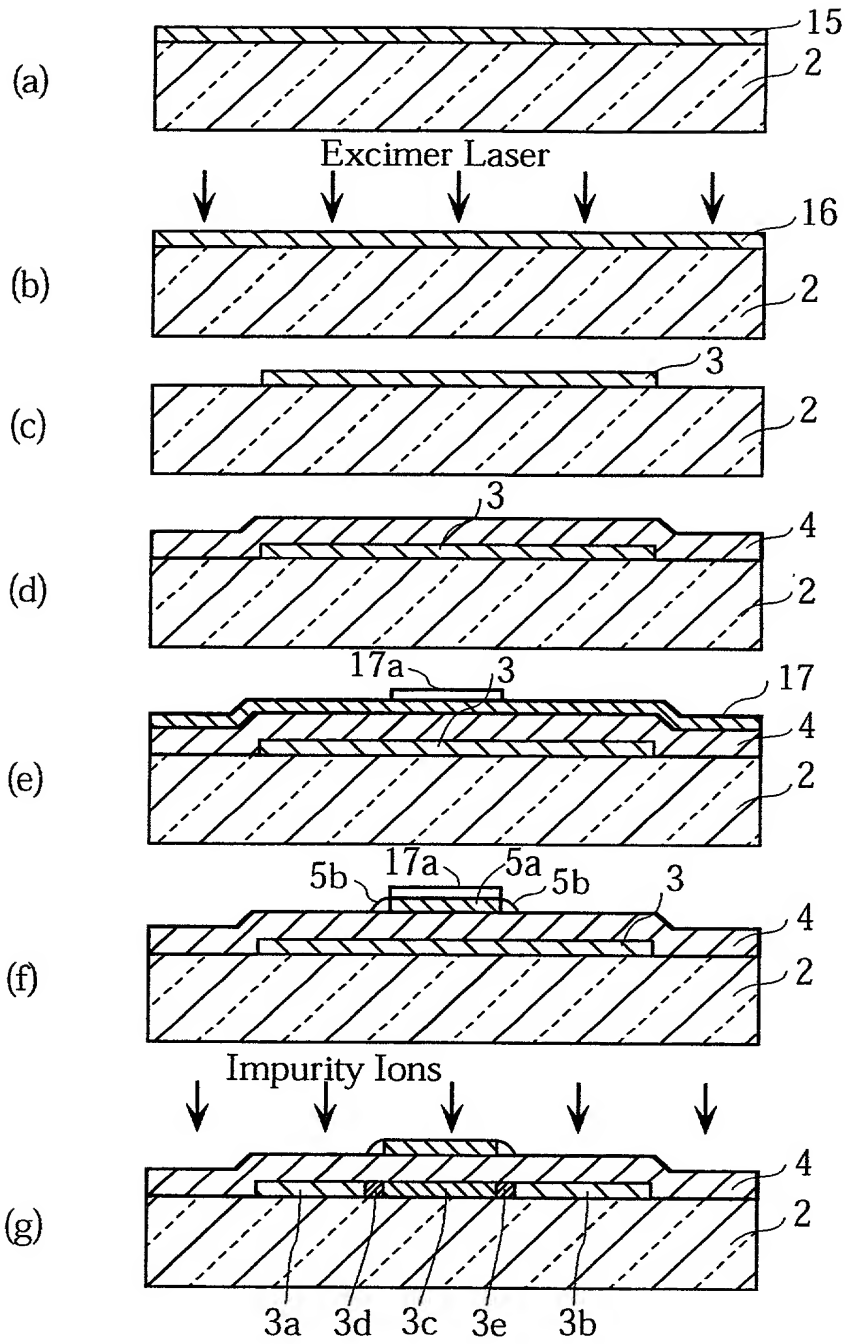

(a)
15
2
Excimer Laser
(b)
16
2
(c)
3
2
(d)
3
4
2
(e)
17a
3
17
4
2
(f)
5b
17a
5a
5b
3
4
2
Impurity Ions
(g)
4
2
3a
3d
3c
3e
3b

Fig. 18

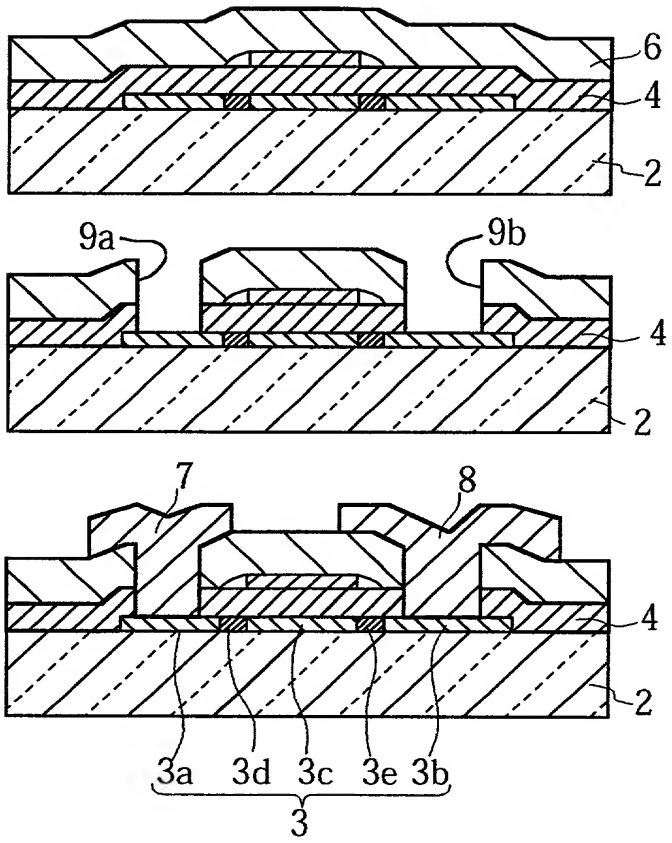


Fig. 19

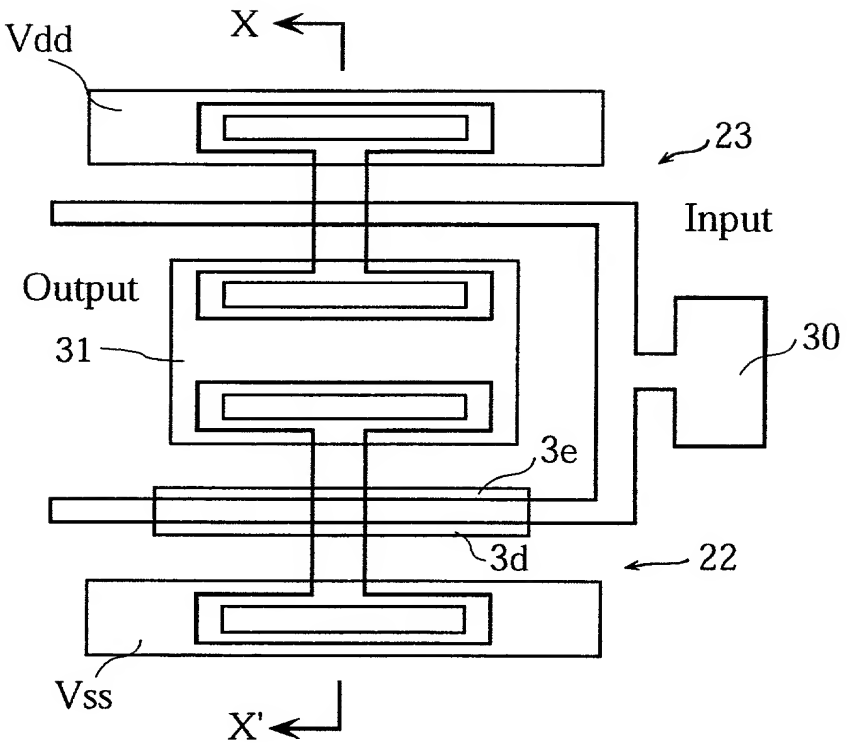
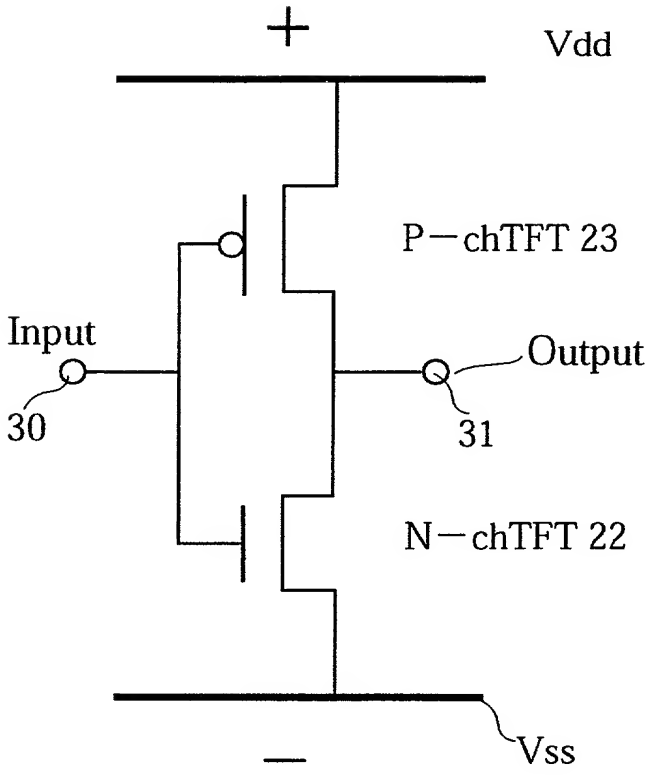


Fig. 20



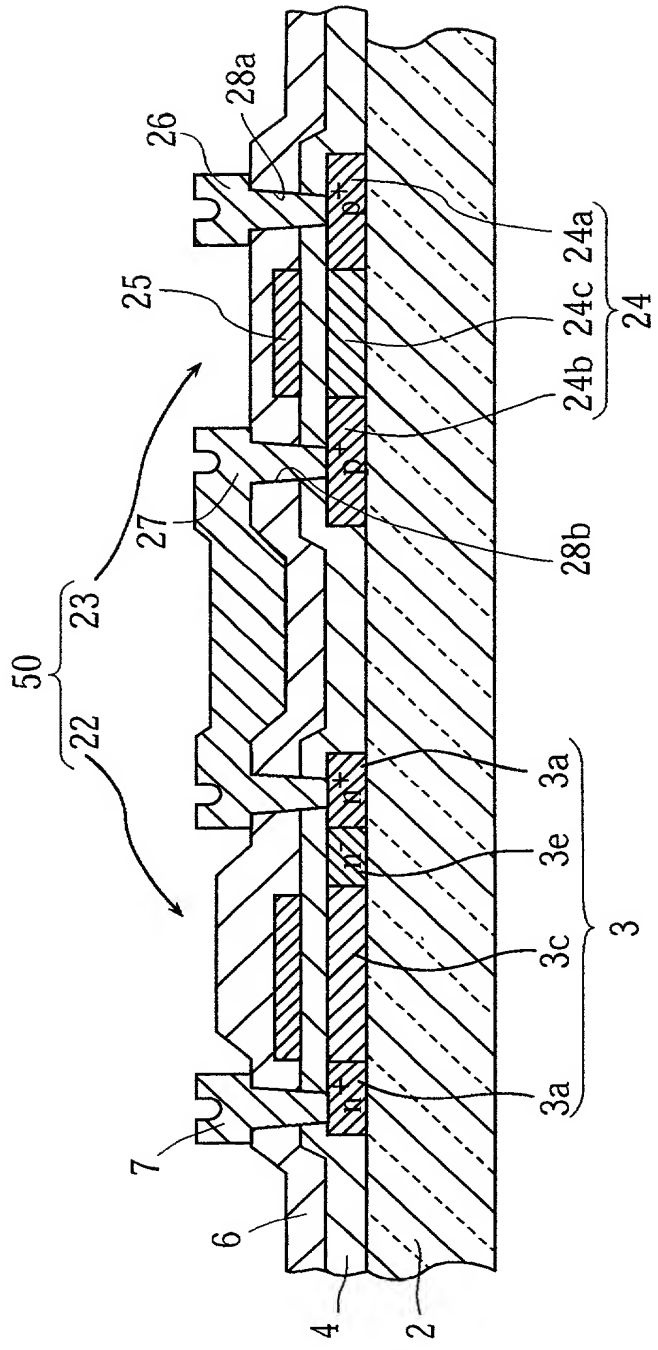


Fig. 21

Fig. 22

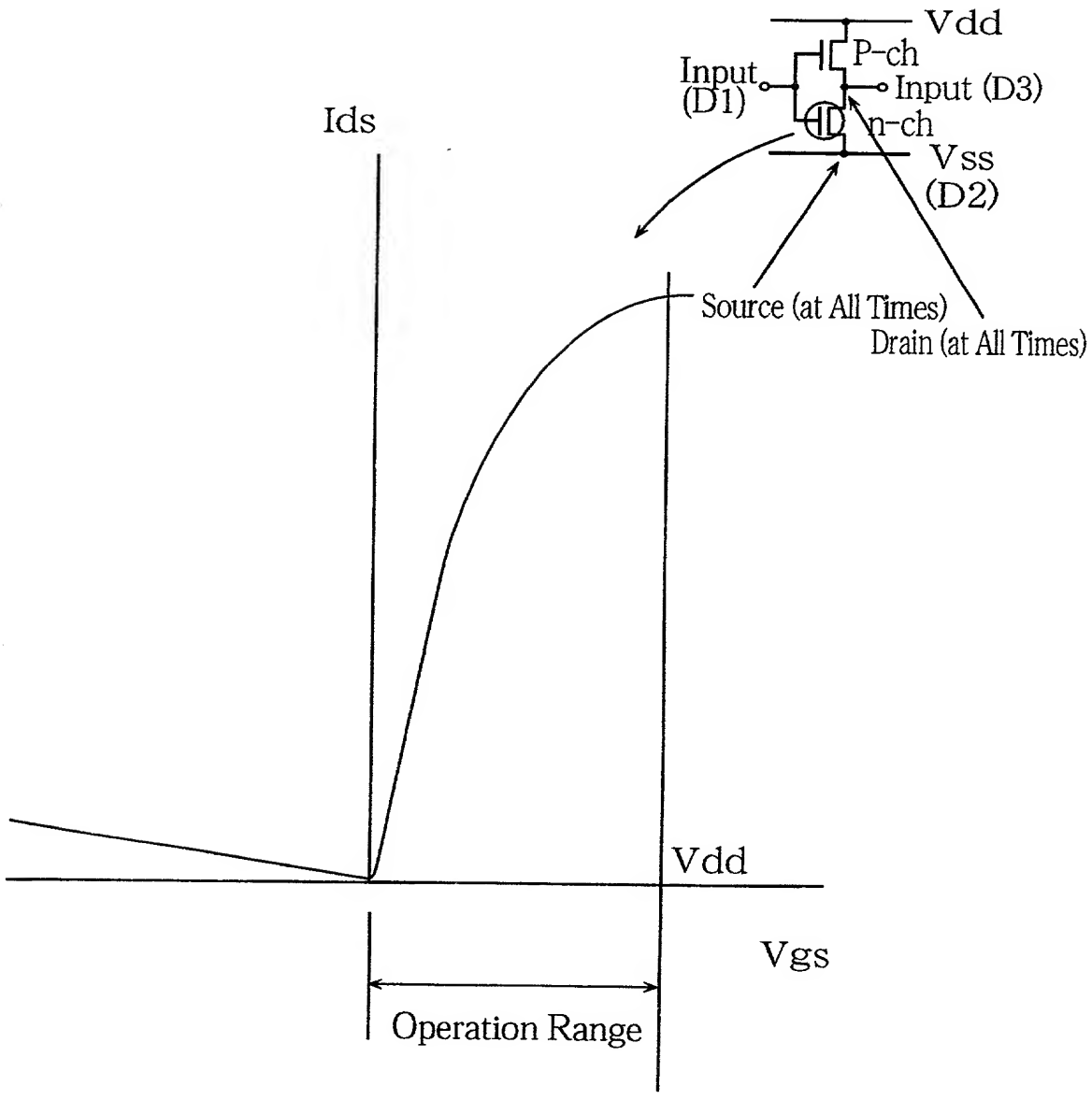

Vdd
P-ch
Input (D3)
Input (D1)
n-ch
Vss (D2)
Ids
Source (at All Times)
Drain (at All Times)
Vdd
Vgs
Operation Range

Fig. 23

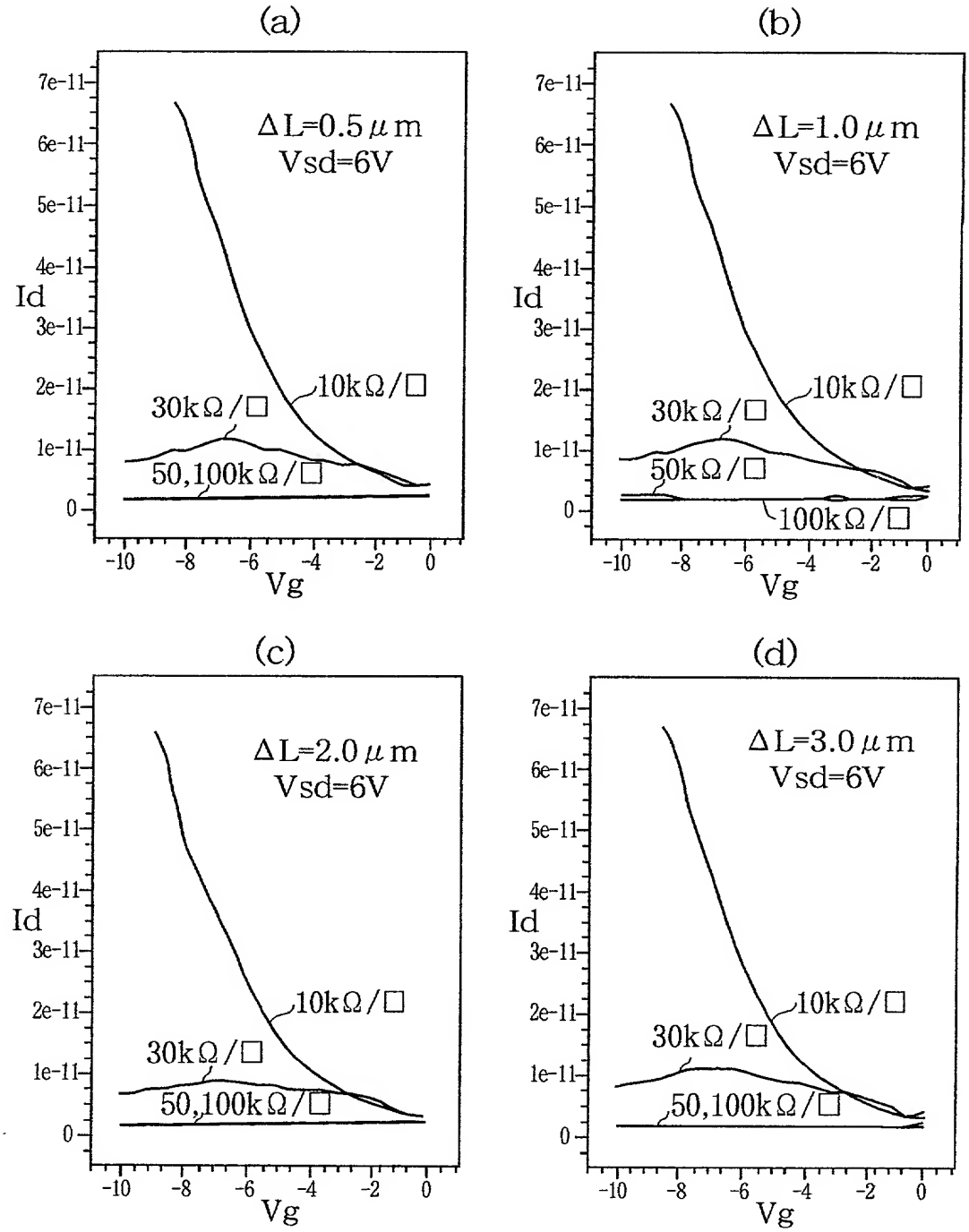
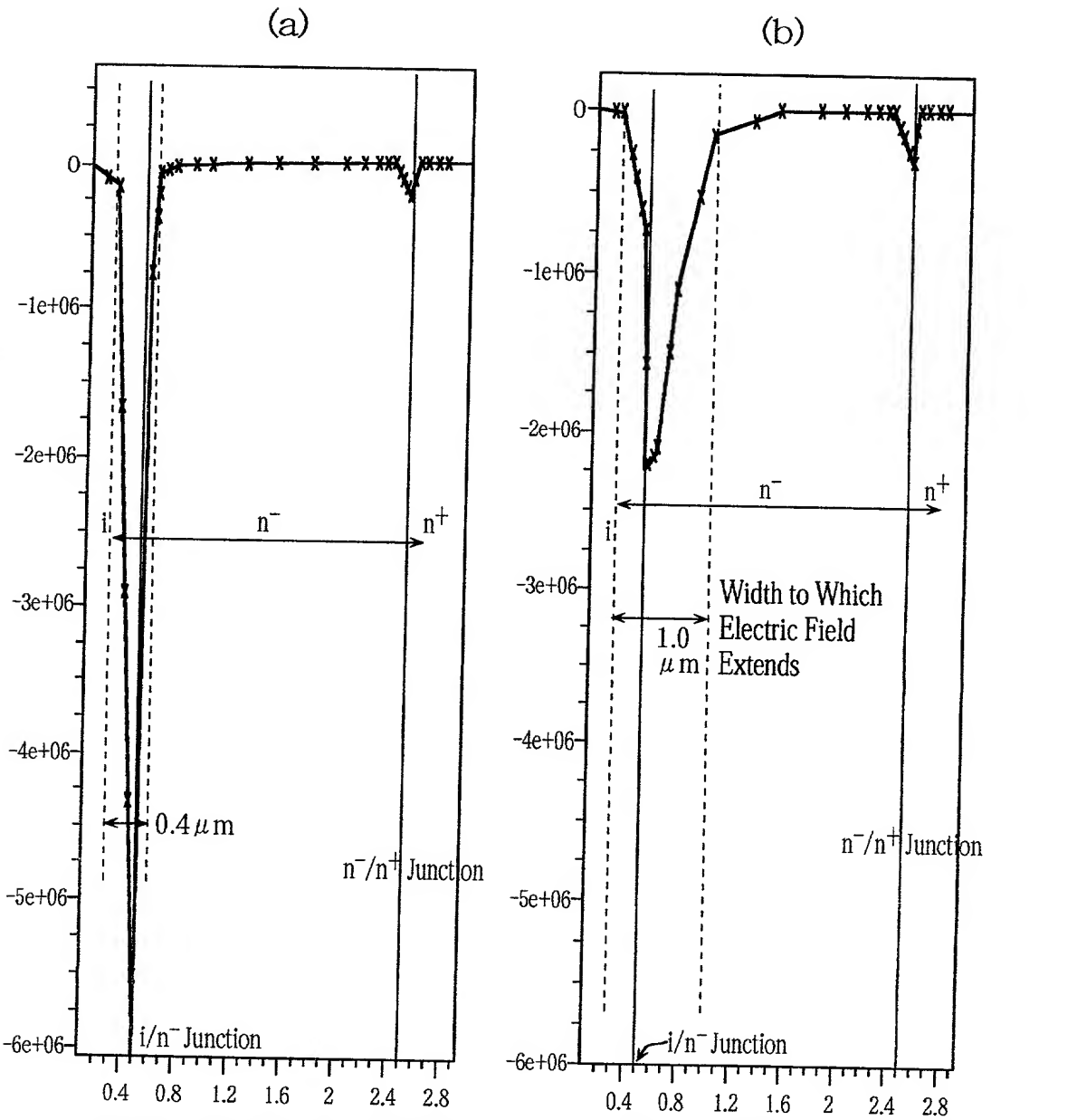

(a)
ΔL=0.5μm
Vsd=6V
10kΩ/□
30kΩ/□
50,100kΩ/□
Id
Vg
(b)
ΔL=1.0μm
Vsd=6V
10kΩ/□
30kΩ/□
50kΩ/□
100kΩ/□
Id
Vg
(c)
ΔL=2.0μm
Vsd=6V
10kΩ/□
30kΩ/□
50,100kΩ/□
Id
Vg
(d)
ΔL=3.0μm
Vsd=6V
10kΩ/□
30kΩ/□
50,100kΩ/□
Id
Vg

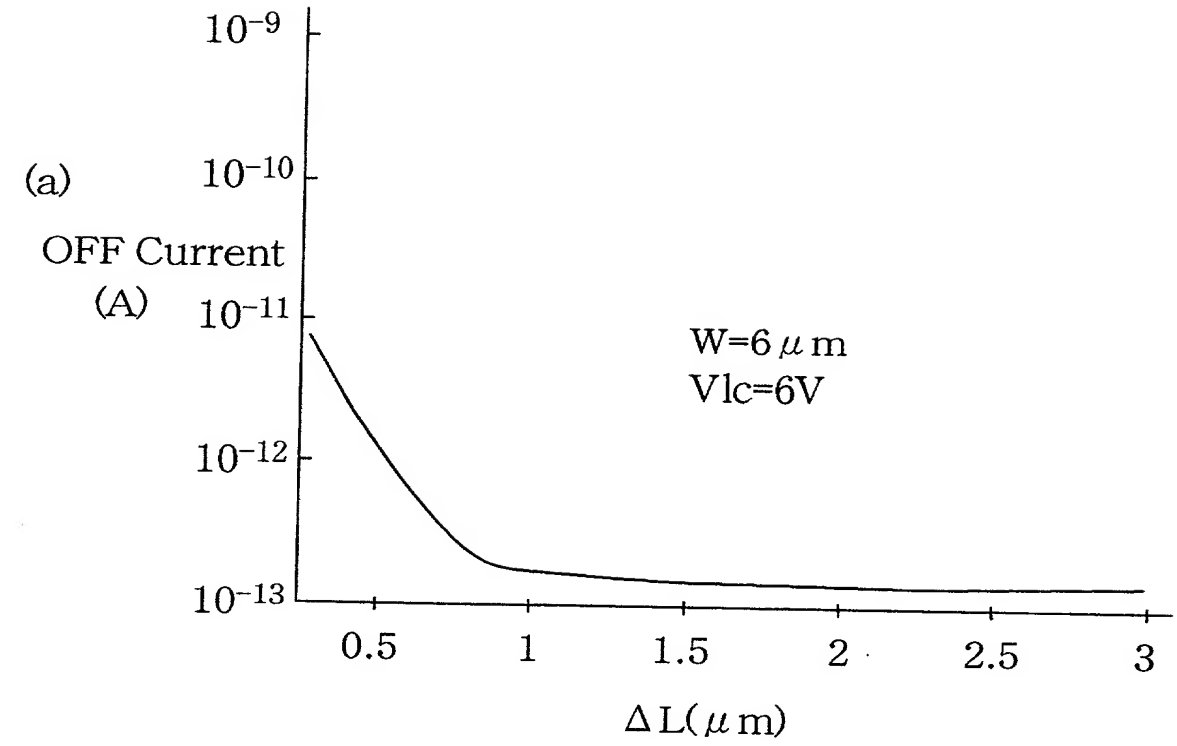
Fig. 24



n⁻ Sheet Resistance 20kΩ/□ n⁻ Sheet Resistance 100kΩ/□

Vg = −10V Vd = 6V

Fig. 25


(a)
OFF Current
(A)
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
W=6 μm
Vlc=6V
0.5
1
1.5
2
2.5
3
ΔL(μm)

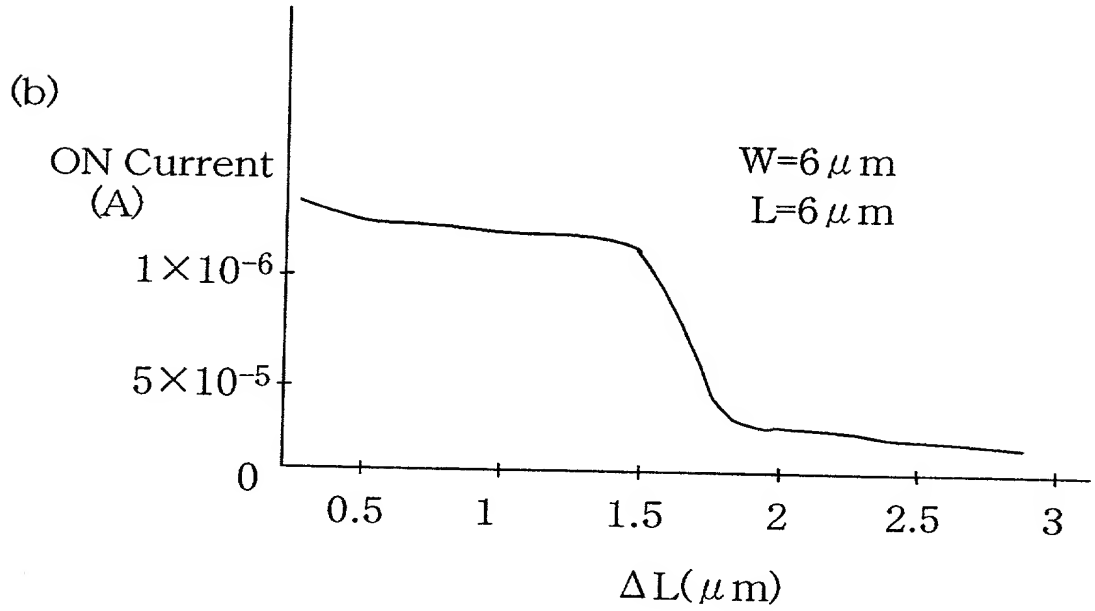

(b)
ON Current
(A)
1×10^{-6}
5×10^{-5}
0
W=6 μm
L=6 μm
0.5
1
1.5
2
2.5
3
ΔL(μm)

Fig. 26

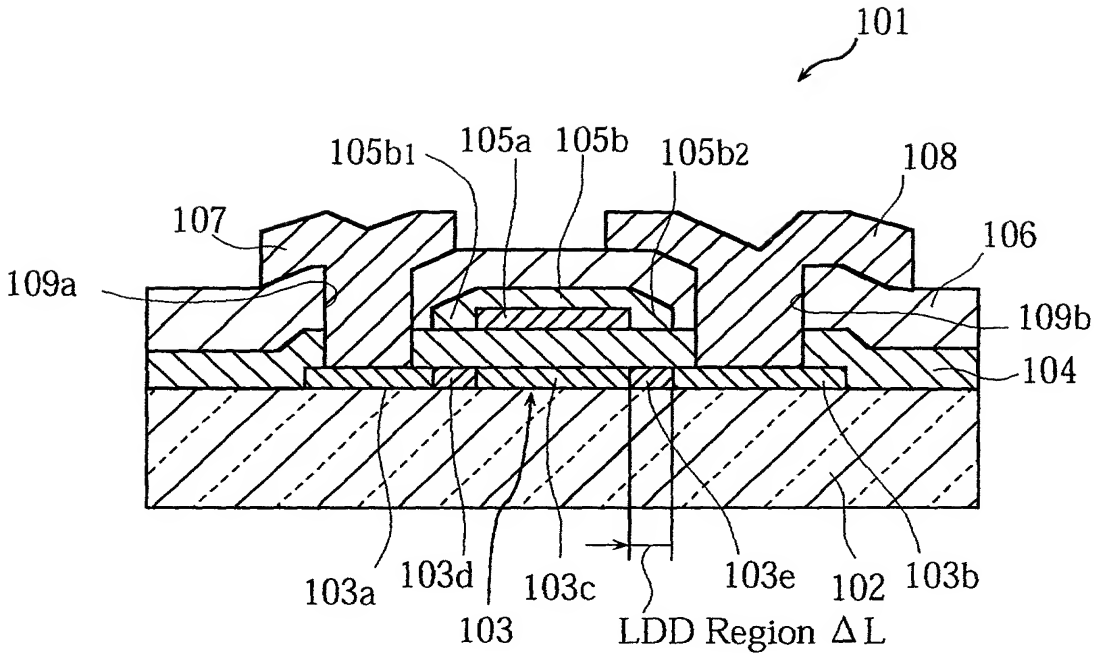

101
105b1
105a
105b
105b2
108
107
106
109a
109b
104
103a
103d
103c
103e
102
103b
103
LDD Region ΔL

Fig. 27

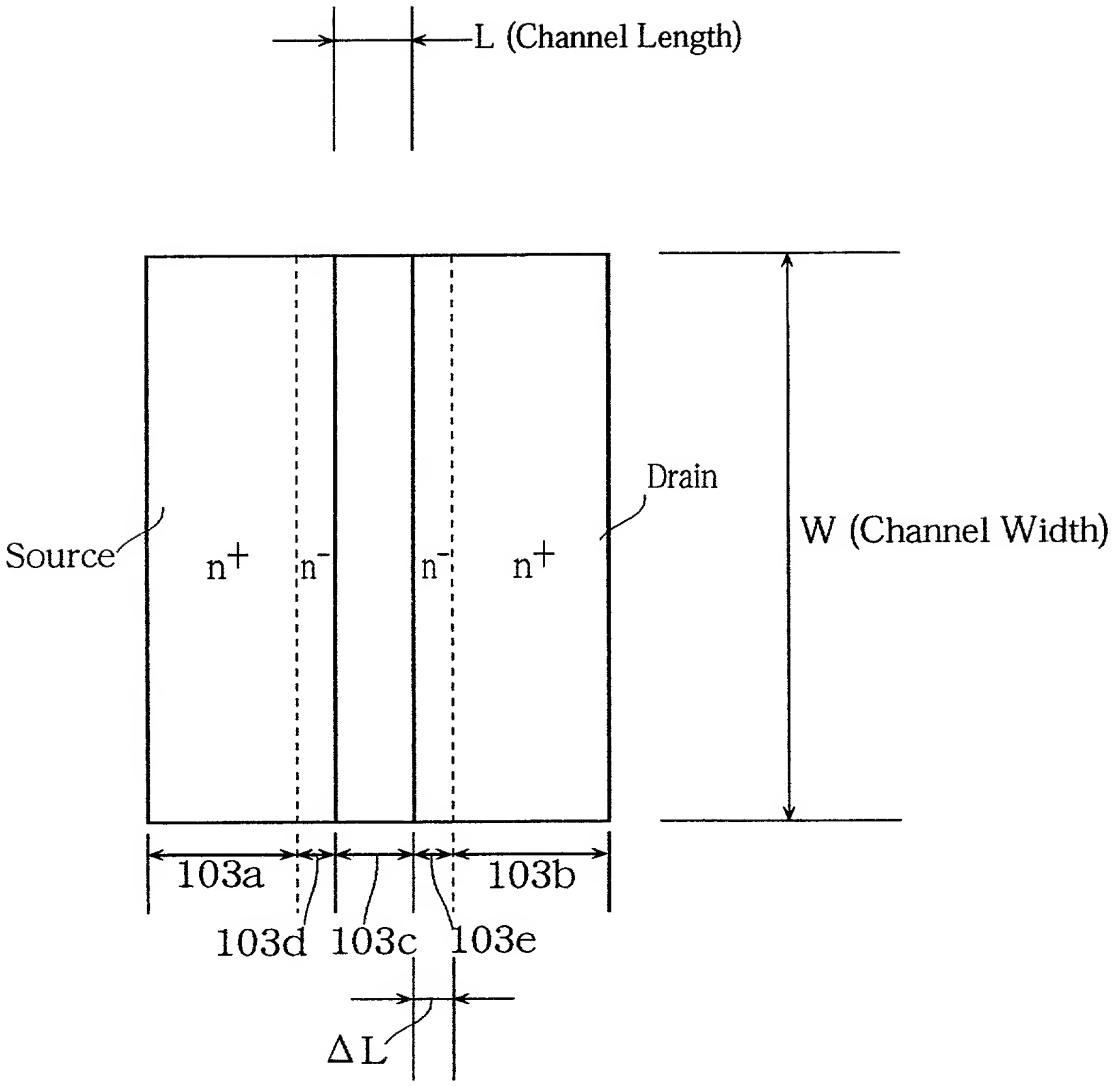

L (Channel Length)
Source
n+
n-
n-
n+
Drain
W (Channel Width)
103a
103b
103d
103c
103e
ΔL

Fig. 28

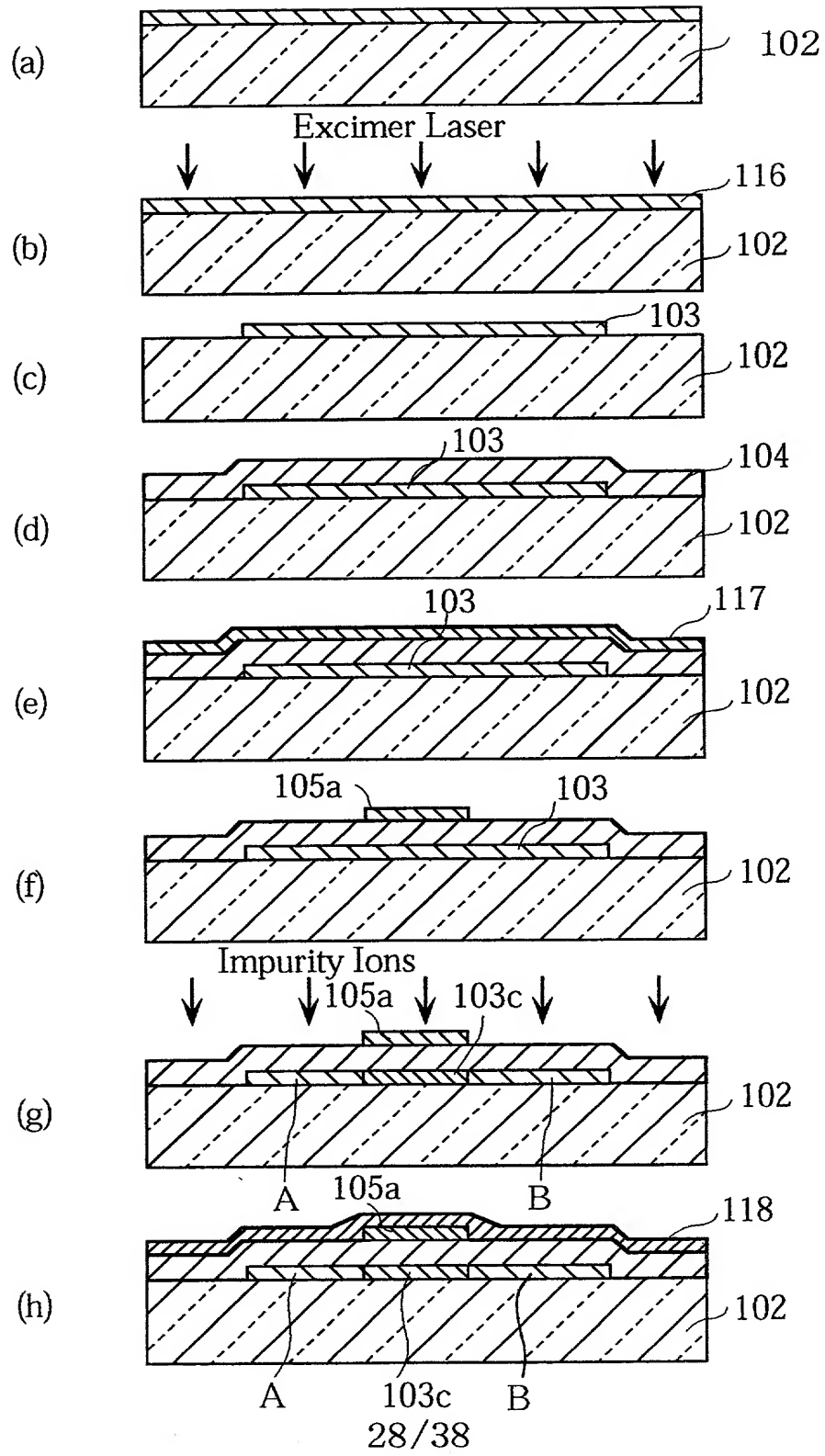

(a)
102
Excimer Laser
116
(b)
102
103
(c)
102
103
104
(d)
102
103
117
(e)
102
105a
103
(f)
102
Impurity Ions
105a
103c
(g)
102
A
105a
B
118
(h)
102
A
103c
B

Fig. 29

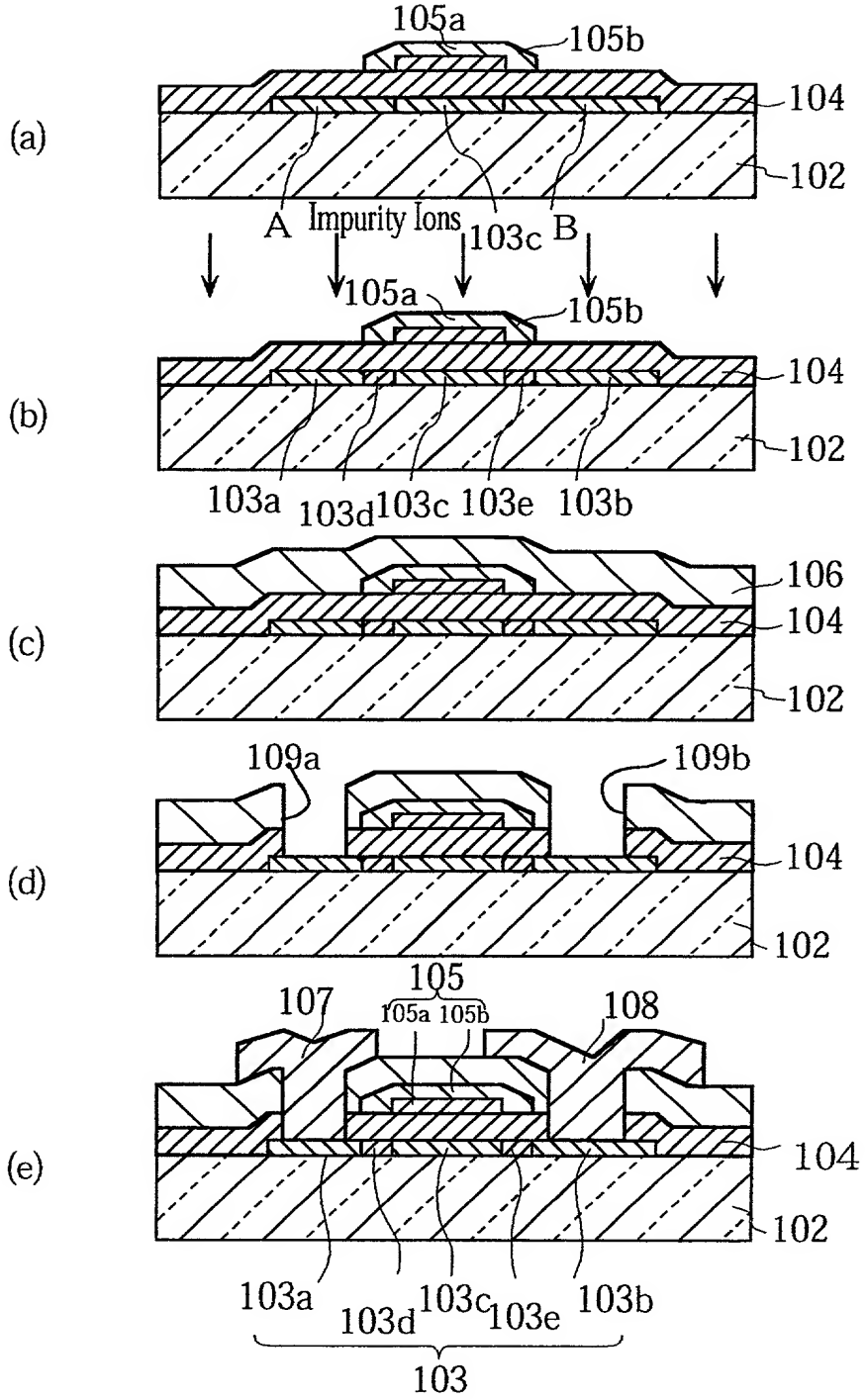

(a)
105a
105b
104
102
A
Impurity Ions
103c
B
(b)
105a
105b
104
102
103a
103d
103c
103e
103b
(c)
106
104
102
(d)
109a
109b
104
102
(e)
105
105a 105b
107
108
104
102
103a
103d
103c
103e
103b
103

Fig. 30

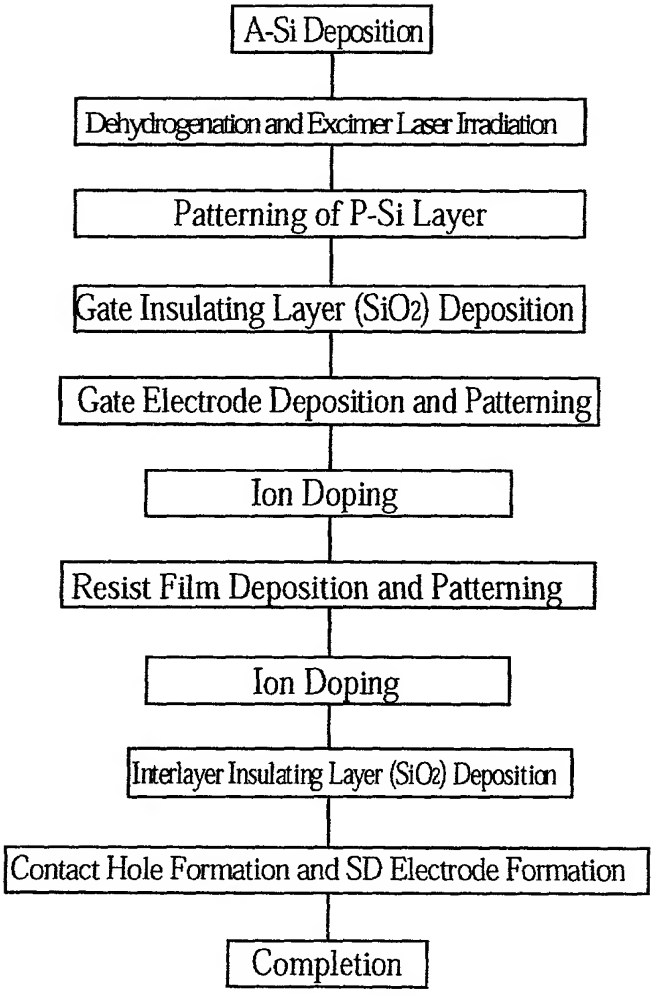

A-Si Deposition
Dehydrogenation and Excimer Laser Irradiation
Patterning of P-Si Layer
Gate Insulating Layer (SiO2) Deposition
Gate Electrode Deposition and Patterning
Ion Doping
Resist Film Deposition and Patterning
Ion Doping
Interlayer Insulating Layer (SiO2) Deposition
Contact Hole Formation and SD Electrode Formation
Completion

Fig. 31

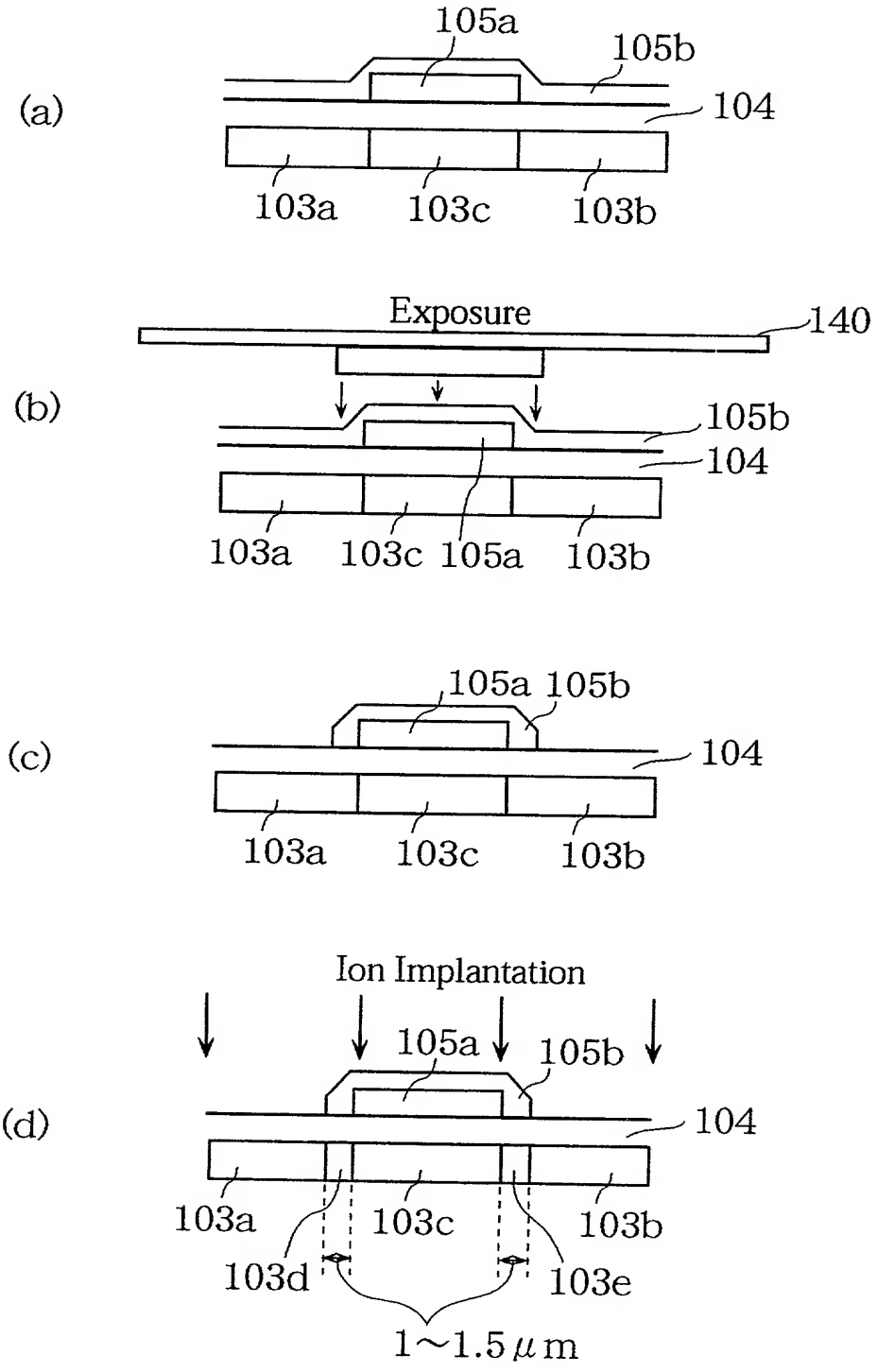

(a)
105a
105b
104
103a
103c
103b
(b)
Exposure
140
105b
104
103a
103c
105a
103b
(c)
105a
105b
104
103a
103c
103b
(d)
Ion Implantation
105a
105b
104
103a
103c
103b
103d
103e
1~1.5μm

Fig. 32

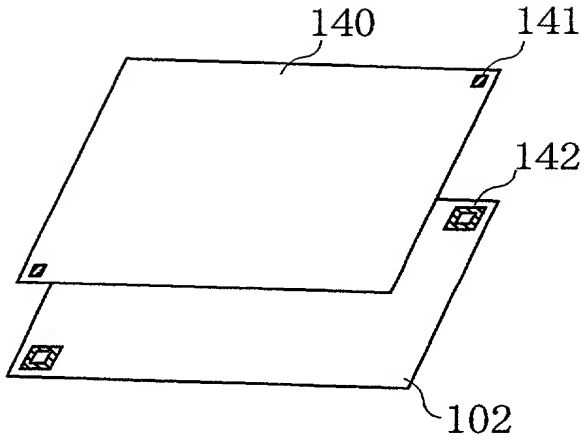


Fig. 33

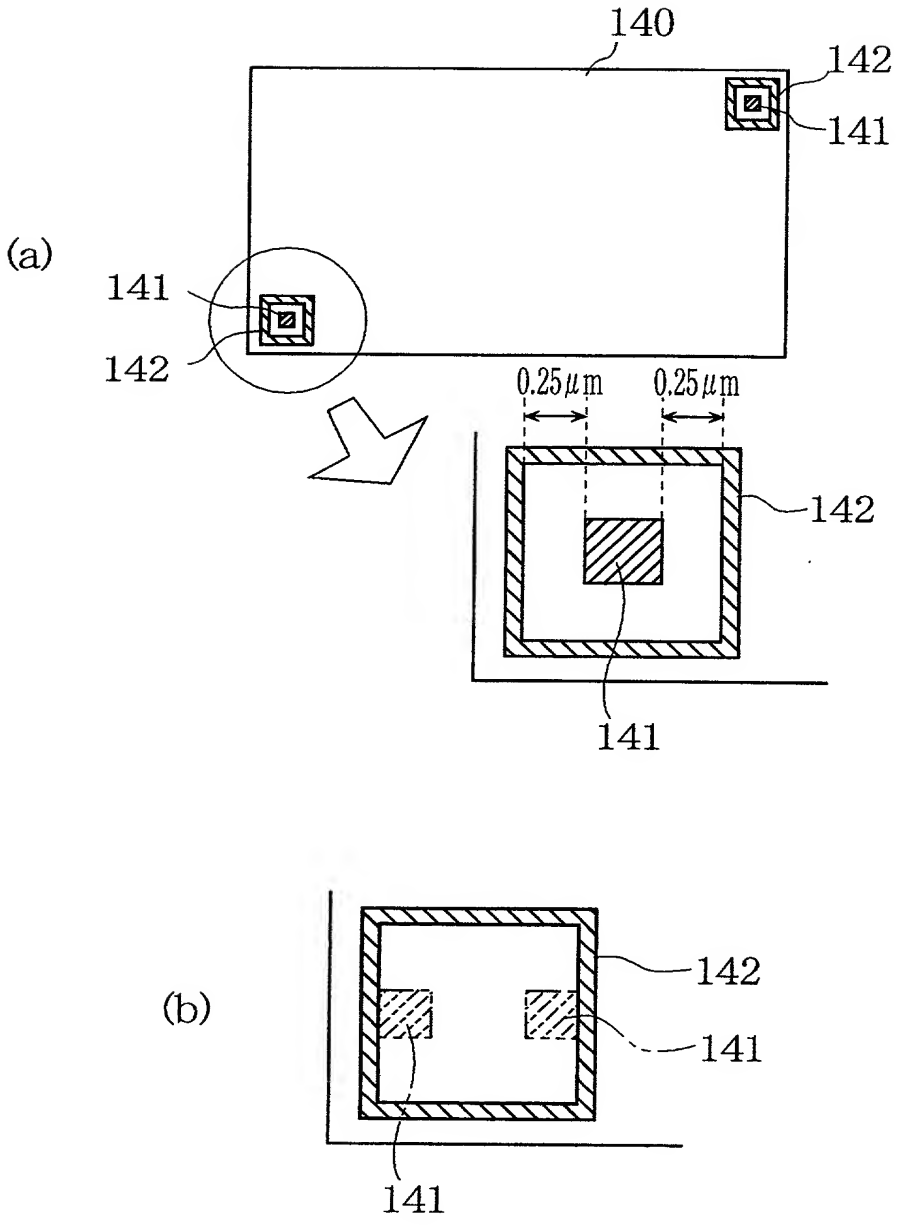
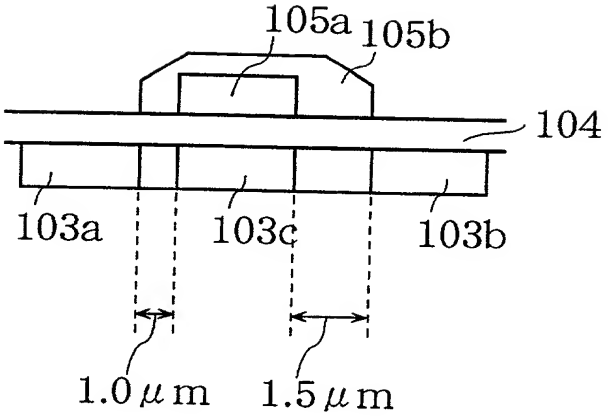


Fig. 34

(a)


105a
105b
104
103a
103c
103b
1.0μm
1.5μm

(b)

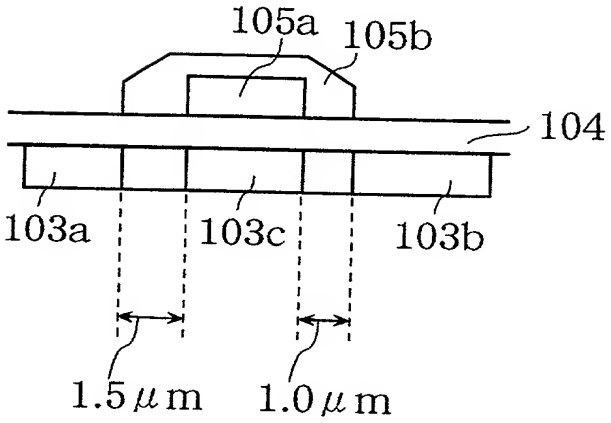

105a
105b
104
103a
103c
103b
1.5μm
1.0μm

Fig. 35

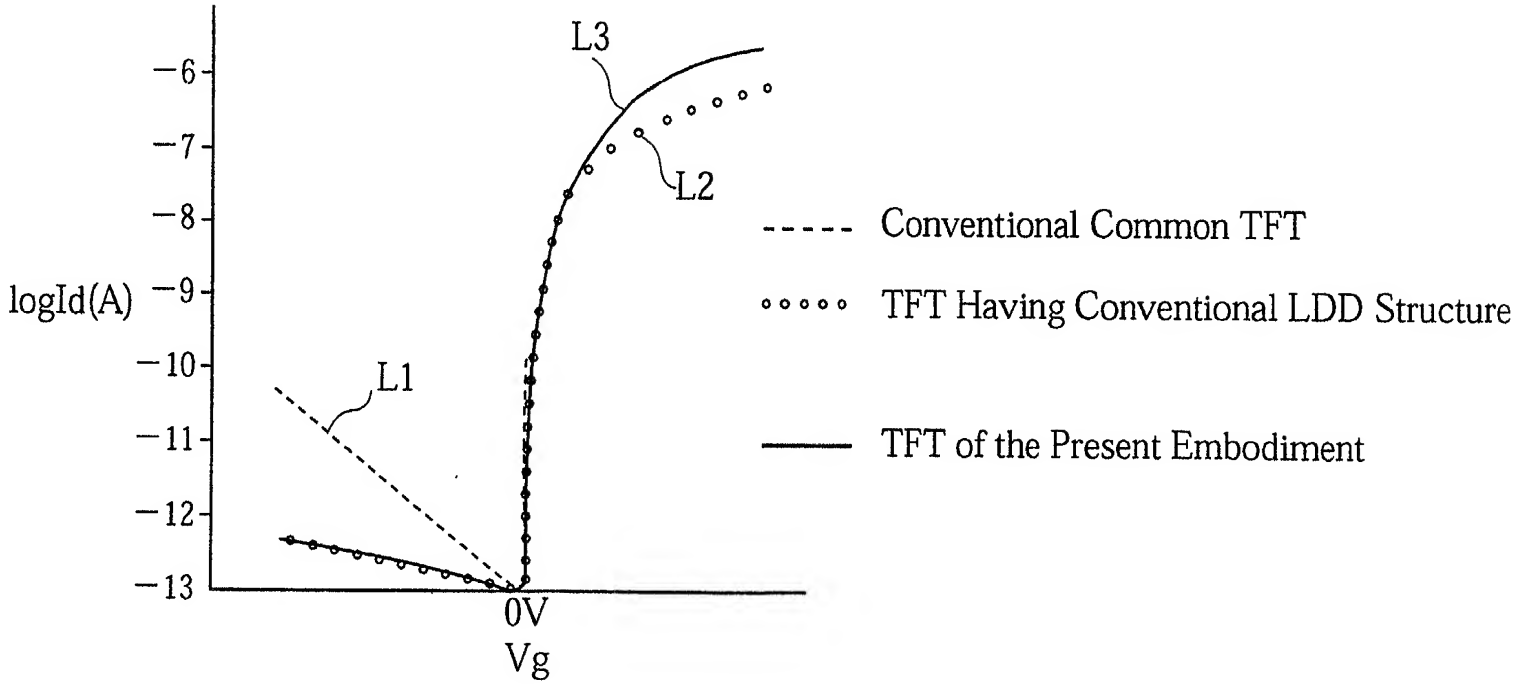


Fig. 36

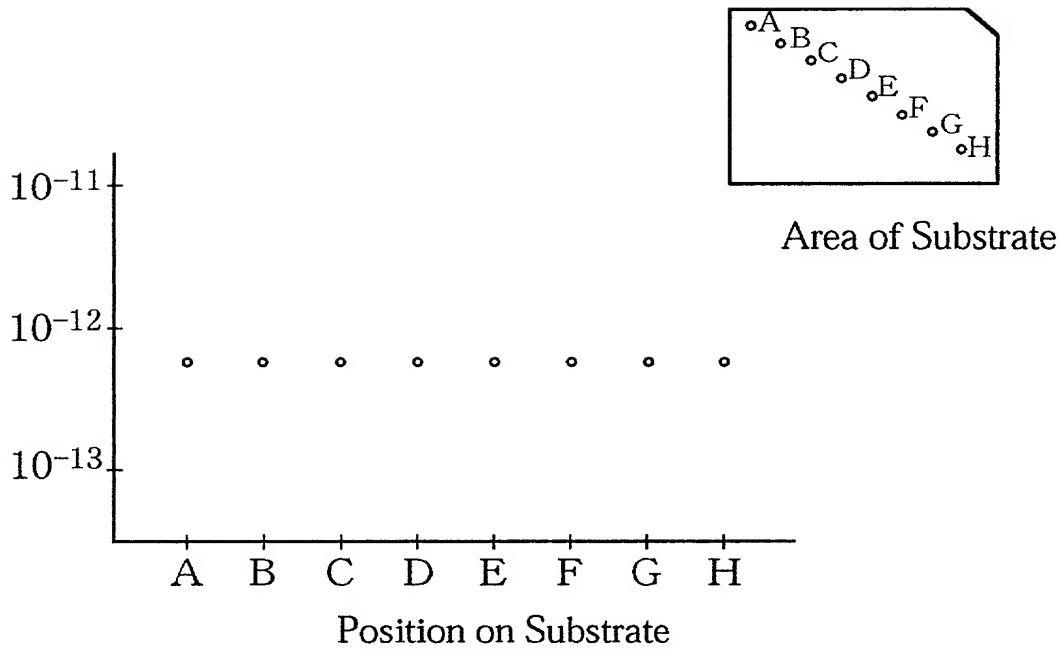

A
B
C
D
E
F
G
H
Area of Substrate
10−11
10−12
10−13
A B C D E F G H
Position on Substrate

Fig. 37

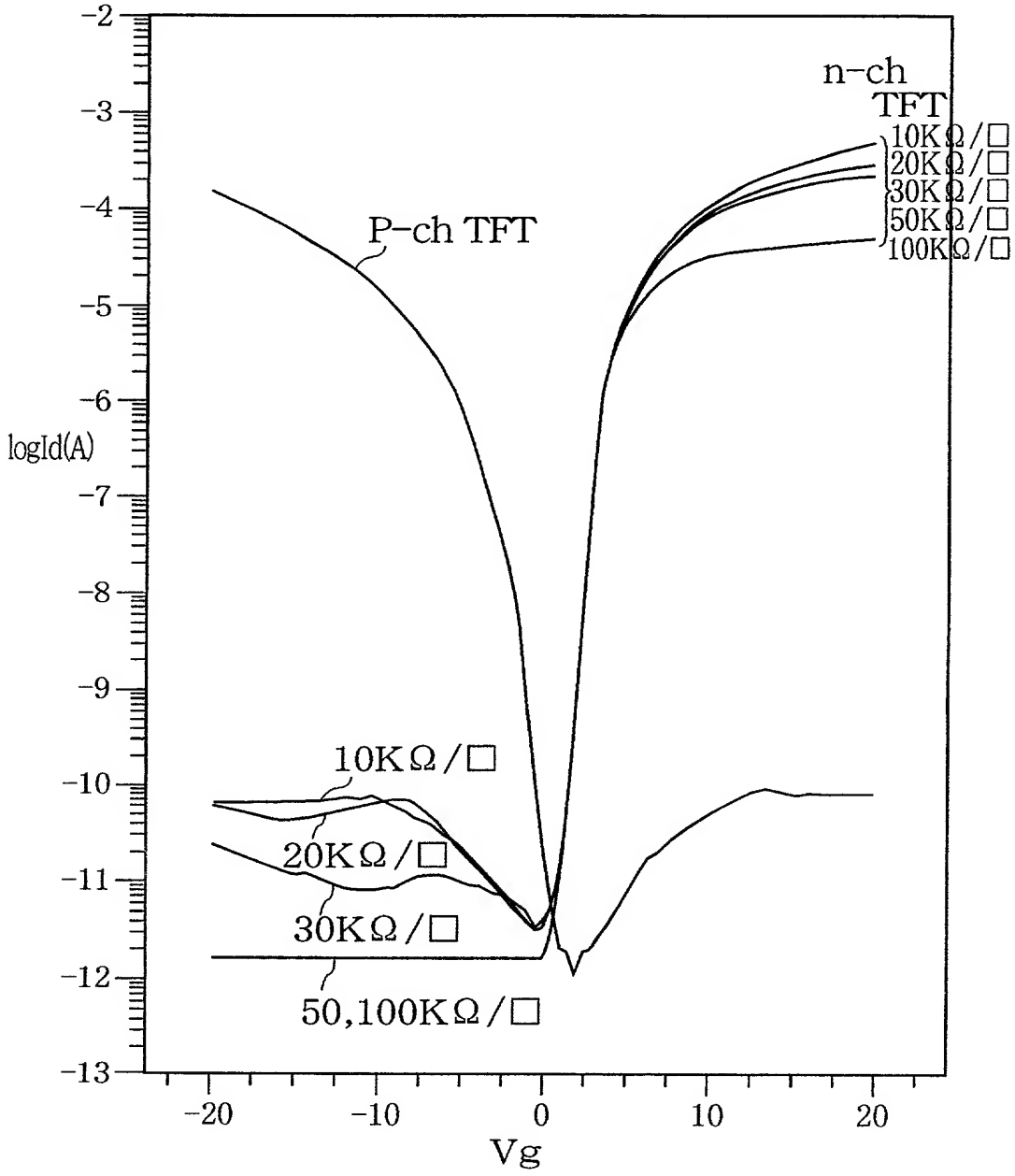
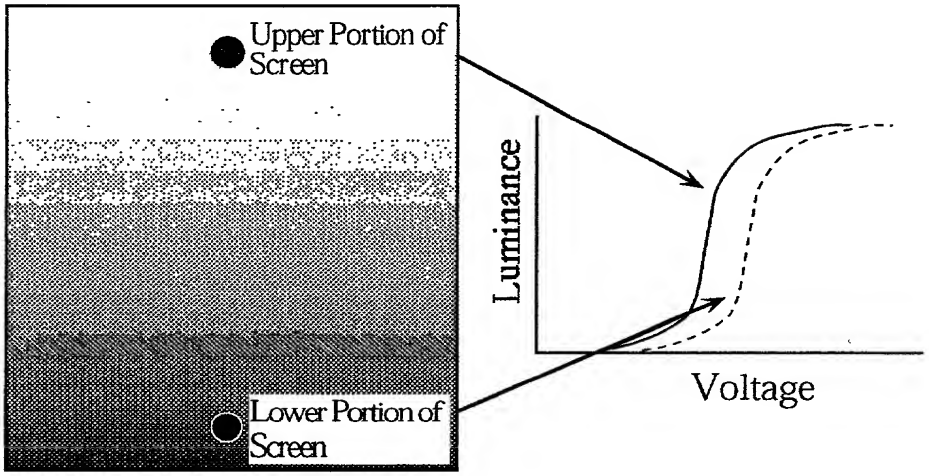
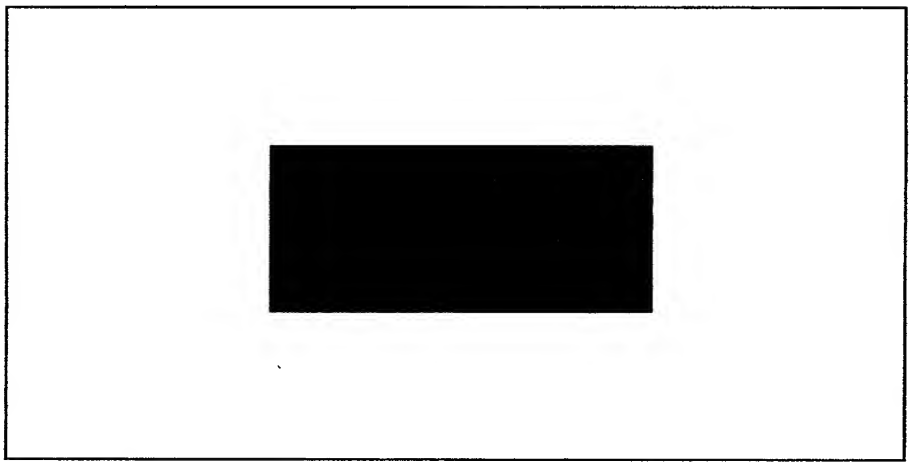

n-ch
TFT
10KΩ/□
20KΩ/□
30KΩ/□
50KΩ/□
100KΩ/□
P-ch TFT
logId(A)
10KΩ/□
20KΩ/□
30KΩ/□
50,100KΩ/□
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-20
-10
0
10
20
Vg

Fig. 38

(a)


Upper Portion of Screen
Lower Portion of Screen
Luminance
Voltage

(b)



Declaration and Power of Attorney
Under Patent Cooperation Treaty
35 USC §371(c)(4)

As a below named inventor, I hereby declare that:

my residence, post office address and citizenship are as stated below next to my name; that

I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural names are named below) of the invention entitled: THIN FILM TRANSISTOR AND METHOD OF PRODUCING THEREOF AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME described and claimed in the international application number PCT/JP00/06330 filed September 14, 2000 and as amended on _____ (if any), the specification and claims of which I have reviewed and understand and for which I solicit a patent.

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a), and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to my international application by me or my legal representatives or assigns, except as follows:

Japanese Patent Application No. 2000-131264 filed on April 28, 2000

Japanese Patent Application No. 2000-197536 filed on June 30, 2000

The priority of the above applications (if any), filed within a year prior to my international application is hereby claimed under 35 USC 119. I hereby appoint the following as my attorneys of record with full power of substitution and revocation to prosecute this application and to transact all business in the patent office:

Roger W. Parkhurst, Reg. No. 25,177; Charles A. Wendel, Reg. No. 24,453; Lawrence D. Eisen, Reg. No. 41,009.

ALL CORRESPONDENCE IN CONNECTION WITH THIS APPLICATION SHOULD BE SENT TO: PARKHURST & WENDEL, L.L.P., 1421 PRINCE STREET, SUITE 210, ALEXANDRIA, VIRGINIA 22314-2805, TELEPHONE (703) 739-0220.

I hereby declare that I have reviewed and understand the contents of this Declaration, and that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

3. Full Name of Sole or First Inventor: Yutaka (Given Name) | (Middle Initial) | NANNO (Family Name)

*4. Inventor's Signature: ☞ Yutaka Nanno

Date of Signature: ☞ November 8. 2001 (Month / Day / Year)

6. Residence: Takarazuka-shi (City) | Hyogo (State or Province) | JAPAN JPX (Country)

7. Citizenship: Japanese

8. Post Office address (Insert complete mailing address, including country): 1-7-1-714, Sakasedai, Takarazuka-shi, Hyogo 665-0024 JAPAN

*IF THERE IS MORE THAN ONE INVENTOR USE PAGE 2 AND PLACE AN "X" HERE ☒.

PAGE 2 OF U.S.A. DECLARATION FORM

(Discard this page in a sole inventor application)

2-00

3 Typewritten Full Name of Second Joint Inventor (if any): Takashi (Given Name) | (Middle Initial) | OKADA (Family Name)

*4 Inventor's Signature: Takashi Okada

5 Date of Signature: November 8, 2001 (Month / Day / Year)

6 Residence: Shijonawate-shi (City) | Osaka (State or Province) | JAPAN JPX (Country)

7 Citizenship: Japanese

8 Post Office Address (Insert complete mailing address, including country): 2-7-12, Minamino, Shijonawate-shi, Osaka 575-0021 JAPAN

3-00

3 Typewritten Full Name of Third Joint Inventor (if any): Atsunori (Given Name) | (Middle Initial) | YAMANO (Family Name)

*4 Inventor's Signature: Atsunori Yamano

5 Date of Signature: November 8, 2001 (Month / Day / Year)

6 Residence: Kawanishi-shi (City) | Hyogo (State or Province) | JAPAN JPX (Country)

7 Citizenship: Japanese

8 Post Office Address (Insert complete mailing address, including country): 2-26-5, Daiwahigashi, Kawanishi-shi, Hyogo 666-0111 JAPAN

4-00

3 Typewritten Full Name of Fourth Joint Inventor (if any): Kouji (Given Name) | (Middle Initial) | SENDA (Family Name)

*4 Inventor's Signature: Kouji Senda

5 Date of Signature: November 8, 2001 (Month / Day / Year)

6 Residence: Nagaokakyo-shi (City) | Kyoto (State or Province) | JAPAN JPX (Country)

7 Citizenship: Japanese

8 Post Office Address (Insert complete mailing address, including country): 12-13, Shimokaiinjikawamukai, Nagaokakyo-shi, Kyoto 617-0845 JAPAN

3 Typewritten Full Name of Fifth Joint Inventor (if any): (Given Name) | (Middle Initial) | (Family Name)

*4 Inventor's Signature:

5 Date of Signature: (Month / Day / Year)

6 Residence: (City) | (State or Province) | (Country)

7 Citizenship:

8 Post Office Address (Insert complete mailing address, including country):

*Note to Inventors: Please sign name on line 4 exactly as it appears in line 3 and insert the actual date of signing on line 5.

**This form may be executed only when attached to the first page of the Declaration and Power of Attorney form and the specification (including claims) of the application to which it pertains.